

Model Name: GA-Z77X-UD5H

rev 1.1

SHEET

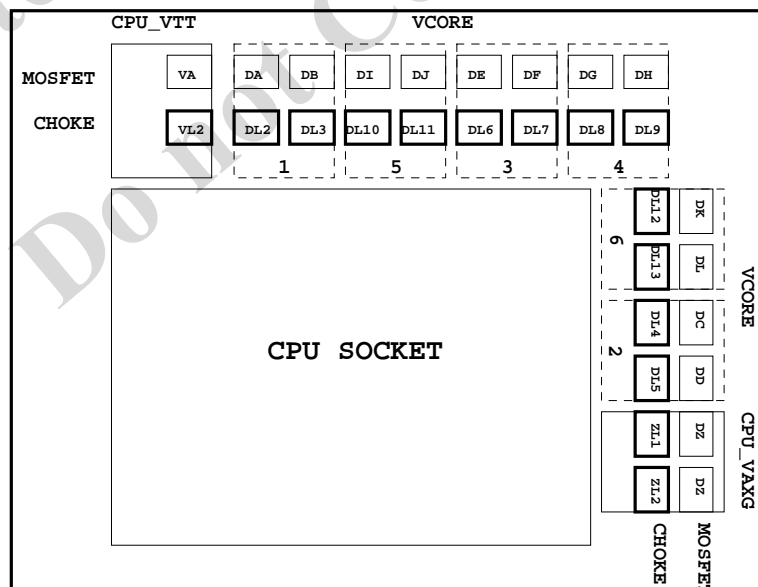
TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*16/*8/*4 SWITCH
18	PCI EXPRESS*1 SLOTS X3
19	ITE 8892
20	PCI SLOT 1
21	HDMI / DVI / DP
22	MSATA
23	Dual BIOS
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27	PWM_IR 3567A
28	IR 3598-VCORE POWER
29	IR 3598-VAXG POWER
30	PWM_IR 3570A
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32	DISCRETE POWER I

SHEET

TITLE

33	VCCSA POWER
34	I/O ITE8728
35	F_PANEL , F_USB , -PHOT
36	F_USB3.0
37	ATX POWER, CLOCK GEN
38	HWM,KB/MS , FAN CTRL
39	ARTHEROS AR8161/AR8151
40	INTEL 82579V
41	Marvell 9172(F+R)
42	Marvell 9172(F)
43	VT6308P 1394
44	VL810 USB3_HUB1(R)
45	VL810 USB3_HUB1(F)
46	RST, PWR, CLR_CMOS
47	TABLE LIST
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Gigabyte Technology

Title			
Cover Sheet			
Size	Document Number	GA-Z77X-UD5H	Rev
Custom			1.1
Date:	Friday, June 01, 2012	Sheet	1 of 47

Component value change history

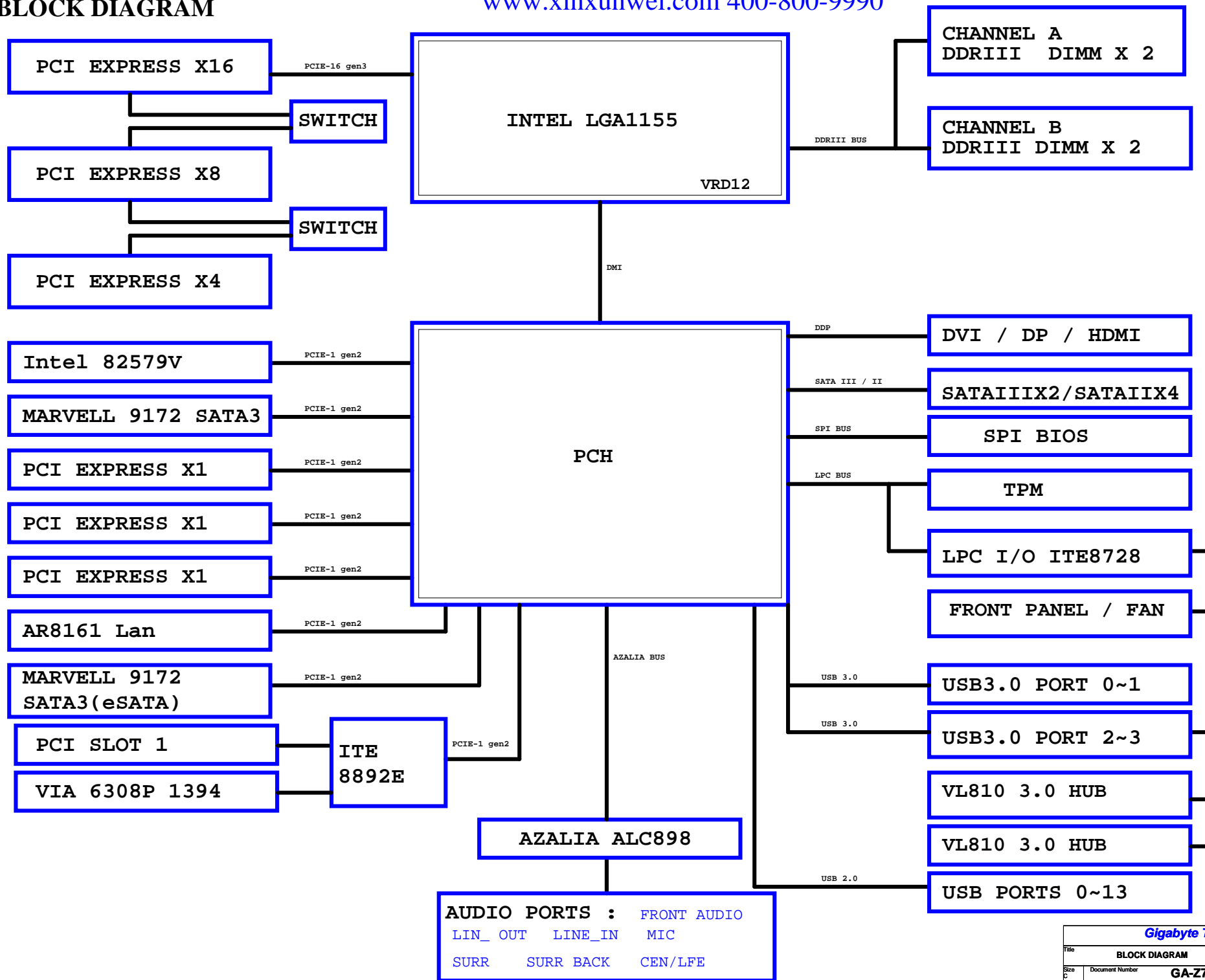
Data	Change Item	Reason
2011/02/10	0.2A	
	REMOVE Amplifier _ISL54405	
2012/01/03	1.0A-EBOM	
	Vcore 改 上1下2	
	IT8892改FX	
	Vcore, VTT, Vaux circuit modify =>remove 3931	
2012/01/18	1.0	
	修改值for Magntiude Response高頻高於-1dB	
	改+12v driver piull high R=>0ohm	
	Q41=>MODIFY : SIR840DP/N/5.4m/PPAKSO-8/[10IF9-040393-01R] for on/off charge	
2012/01/19	1.01B	
	修改 PCB 文字面 "SYS_FAN 1", "SYS_FAN 2", "SYS_FAN 3""SYS_FAN 4"	
2012/01/30	1.01C	
	改PROCHOT 阻值	
	改driver端0 ohm to 5v	
	改choke : 0.36uH/38A/IGC109/FS/D/[11LC5-F3360B-01R]	
2012/02/03	1.01D	
	FOR Vcore and Vaux bom modify	
	For dvi test add HR83	
2012/03/05	1.01E	
	ADD HR147 HR148 FOR VIA HUB USB3 LOSS ISSUE ;	
	ADD MB_ID2 ; H : VIA HUB reset L : 1.01	
2012/03/06	1.02J	
	ADD CPU CFG9 CTRL	
	ADD DBC126 for EMI	
	ADD MB_ID3 H:Rev1.02	
	ADD MR14,MBC34,MBC35,MBC36,MR15	
2012/03/22	1.03K	
	Modify PCB	
2012/04/20	1.03N	
	Change to IR 3567A (DAU1),Del DAESD1,3570A (MAU40)	
	8728 SIO_18V Change to 0.1uF	
	AUDIO AP w/ inbox driver	
2012/05/09	MB_ID2 OR7->OR15	
2012/06/05	1.1A	
	LAN change to Atheros 8161 , LAR1->1%	
	Add GPIO17 , GPIO1 MB_ID , PCH Core R131-> X , R132->0	
	F.B 30,60 down size ,ATX PWOK Add 4.7u/6/X5R/6.3V/K + 0 ohm	
	Footprint ATX->ATXPWR_24-6 , ATX_12V_2X4->ATXPW2X4-6	
	R199->10K , R198->499 , change N_GPIO38 to standby pin,Add PR5 & OR173	
	VEC3 ,VEC4,VEC5 Change to 820u	
	IESD3 pin 5 change to FUSEVCC3,LGA1155 change to 12KRC-0F0001-23	
	VCORE,VAXG,DDR_15V,CPU_VTT Low size MOS and Q41 change to 10IF9-040393-11R	
	CFB2,LAFB3,CFB3,LAFB2,LAR5,RHFB2,RIFB2,change to 0402	
2012/07/25	1.1B	
	R191->12.7K PCH core Add 50mV , Del HP_PWR	

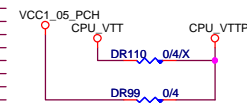
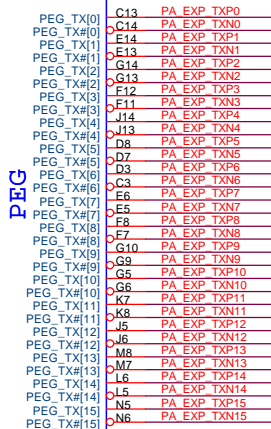
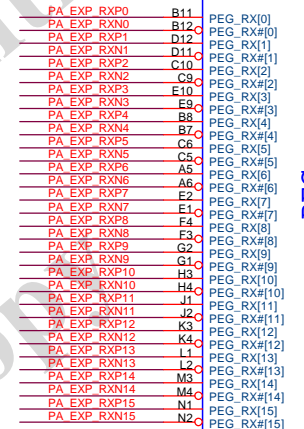
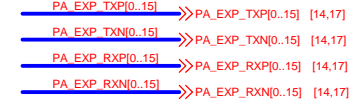
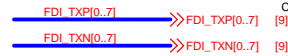
Circuit or PCB layout change

DATE	Change Item	Reason
2012/01/19	REV1.01 修改 PCB 文字面 "SYS_FAN 1", "SYS_FAN 2", "SYS_FAN 3""SYS_FAN 4"	
2012/03/02	REV1.02 修改DDR部分	
2012/03/21	REV1.03 修改文字面	
2012/06/04	REV1.1 Add GPIO17 , GPIO1 MB_ID F.B 30,60 down size ,ATX PWOK Add 4.7u/6/X5R/6.3V/K + 0 ohm Footprint ATX->ATXPWR_24-6 , ATX_12V_2X4->ATXPW2X4-6 change N_GPIO38 to standby pin,Add PR5 & OR173 IESD3 pin 5 change to FUSEVCC3 CFB2,LAFB3,CFB3,LAFB2,LAR5,RHFB2,RIFB2,change to 0402	

# BLOCK DIAGRAM

www.xinxunwei.com 400-800-9990



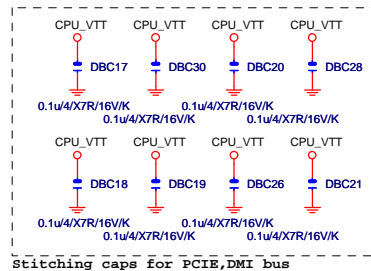
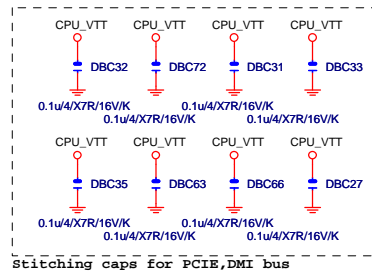
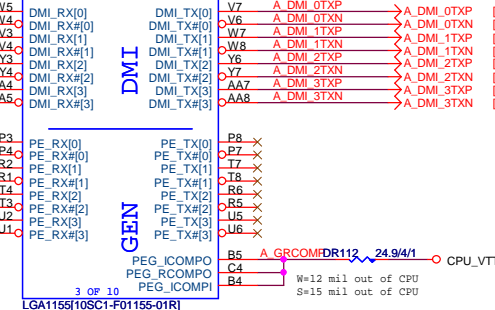
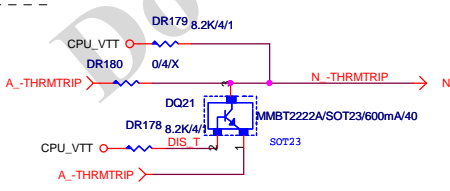


CFG6	CFG5	PCIE CONFIG
1	1	1x16 , Default
1	0	2X8
0	1	RSVD
0	0	X8,X4,X4

Schematic diagram of the power supply section for the AD9288. The diagram shows the following components and connections:

- N\_DRAM\_PWROK** signal connected to a pull-up resistor **R\_15V** (100/4/1) and a diode **DBC34** (100p4/NPO/50V/J/X) to ground.
- A\_SM\_VREF** signal connected to a diode **DBC78** (0.1u4/X7R/16V/K) to ground and a resistor **DR182** (0/4/SHT/X) to the **A\_SMREF\_ADJ** pin [46].
- A\_THR** signal connected to a diode **DB1** (0.1u4/X7R/16V/K/X) to ground.
- A dashed box highlights the **PCH\_GP45** pin [12] connected to the **DIS\_T** signal.

[9]	A_DMI_0RXP	A_DMI_0RXP	W5
[9]	A_DMI_0RXN	A_DMI_0RXN	W4
[9]	A_DMI_1RXP	A_DMI_1RXP	V3
[9]	A_DMI_1RXN	A_DMI_1RXN	V4
[9]	A_DMI_2RXP	A_DMI_2RXP	Y3
[9]	A_DMI_2RXN	A_DMI_2RXN	Y4
[9]	A_DMI_3RXP	A_DMI_3RXP	AA4
[9]	A_DMI_3RXN	A_DMI_3RXN	AA5



## LGA1155A

M_AA0	AV27	SA_MA[0]	SA_DQS[0]	AK3	M_DQSA0
M_AA1	AY24	SA_MA[1]	SA_DQS[0]	AK2	M_DQSA0
M_AA2	AW24	SA_MA[2]			
M_AA3	AW23	SA_MA[3]			
M_AA4	AV23	SA_MA[4]	SA_DQ[0]	AJ3	M_DA0
M_AA5	AT24	SA_MA[5]	SA_DQ[1]	AJ4	M_DA1
M_AA6	AT23	SA_MA[6]	SA_DQ[2]	AJ3	M_DA2
M_AA7	AU22	SA_MA[7]	SA_DQ[3]	AL4	M_DA3
M_AA8	AV22	SA_MA[8]	SA_DQ[4]	AJ2	M_DA4
M_AA9	AT22	SA_MA[9]	SA_DQ[5]	AJ1	M_DA5
M_AA10	AV28	SA_MA[10]	SA_DQ[6]	AL2	M_DA6
M_AA11	AU21	SA_MA[11]	SA_DQ[7]	AL1	M_DA7
M_AA12	AT21	SA_MA[12]			
M_AA13	AW32	SA_MA[13]	SA_DQS[1]	AP3	M_DQSA1
M_AA14	AU20	SA_MA[14]	SA_DQS[1]	AP2	M_DQSA1
M_AA15	AT20	SA_MA[15]			

[7]	M_SWEA	AW29	SA_WE#
[7]	M_SCASA	AV30	SA_CAS#
[7]	M_SRASA	AU28	SA_RAS#
[7]	M_SBAA0	AY29	SA_BS[0]
[7]	M_SBAA1	AW28	SA_BS[1]
[7]	M_SBAA2	AV20	SA_BS[2]

[7]	M-CSA0	AU29	SA_CS#
[7]	M-CSA1	AV32	SA_CS#
[7]	M-CSA2	AW30	SA_CS#
[7]	M-CSA3	AU33	SA_CS#

[7]	M-CKEA0	AV19	SA_CKE[0]
[7]	M-CKEA1	AT19	SA_CKE[1]
[7]	M-CKEA2	AU18	SA_CKE[2]
[7]	M-CKEA3	AV18	SA_CKE[3]

	M_ODT_A0	AV31	SA_ODT[0]
	M_ODT_A1	AU32	SA_ODT[1]
	M_ODT_A2	AU30	SA_ODT[2]
	M_ODT_A3	AW33	SA_ODT[3]

[7]	M_DCLKA0	AY25	SA_CK[0]
[7]	M_DCLKA0	AW25	SA_CK[0]
[7]	M_DCLKA1	AU24	SA_CK[1]
[7]	M_DCLKA1	AU25	SA_CK[1]
[7]	M_DCLKA2	AW27	SA_CK[2]
[7]	M_DCLKA2	AY27	SA_CK[2]
[7]	M_DCLKA3	AU26	SA_CK[3]
[7]	M_DCLKA3	AW26	SA_CK[3]

[7,8]	M_DDR3_RST	MR1	SM_DRAMRST#
		MBC8	0.1u/4X7R/16V/K/X

AV13	SA_DQS[8]
AV12	SA_DQS[8]
AU12	SA_ECC_CB[0]
AU14	SA_ECC_CB[1]
AW13	SA_ECC_CB[2]
AY13	SA_ECC_CB[3]
AU13	SA_ECC_CB[4]
AU11	SA_ECC_CB[5]
AY12	SA_ECC_CB[6]
AW12	SA_ECC_CB[7]

DDR\_0

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LGA1155[10SC1-F01155-01R]

## LGA1155B

M_AAB0	AK24	SB_MA[0]	SB_DQS[0]	AH7	M_DQSB0
M_AAB1	AM20	SB_MA[1]	SB_DQS[0]	AH6	M_DQSB0
M_AAB2	AM19	SB_MA[2]			
M_AAB3	AK18	SB_MA[3]	SB_DQ[0]	AG7	M_DB0
M_AAB4	AP19	SB_MA[4]	SB_DQ[1]	AG8	M_DB1
M_AAB5	AP18	SB_MA[5]	SB_DQ[2]	AJ9	M_DB2
M_AAB6	AM18	SB_MA[6]	SB_DQ[3]	AJ8	M_DB3
M_AAB7	AL18	SB_MA[7]	SB_DQ[4]	AG5	M_DB4
M_AAB8	AN18	SB_MA[8]	SB_DQ[5]	AG6	M_DB5
M_AAB9	AY17	SB_MA[9]	SB_DQ[6]	AJ6	M_DB6
M_AAB10	AN23	SB_MA[10]	SB_DQ[7]	AJ7	M_DB7
M_AAB11	AU17	SB_MA[11]			
M_AAB12	AT18	SB_MA[12]	SB_DQS[1]	AM8	M_DQSB1
M_AAB13	AR26	SB_MA[13]	SB_DQS[1]	AL8	M_DQSB1
M_AAB14	AY16	SB_MA[14]			
M_AAB15	AV16	SB_MA[15]			

[8]	M_SWEB	AR25	SB_WE#
[8]	M_SCASB	AK25	SB_CAS#
[8]	M_SRASB	AP24	SB_RAS#
[8]	M_SBAB0	AP23	SB_BS[0]
[8]	M_SBAB1	AM22	SB_BS[1]
[8]	M_SBAB2	AW17	SB_BS[2]

[8]	M-CSB0	AN25	SB_CS#
[8]	M-CSB1	AN26	SB_CS#
[8]	M-CSB2	AL26	SB_CS#
[8]	M-CSB3	AT26	SB_CS#

[8]	M-CKEB0	AU16	SB_CKE[0]
[8]	M-CKEB1	AY15	SB_CKE[1]
[8]	M-CKEB2	AW15	SB_CKE[2]
[8]	M-CKEB3	AV15	SB_CKE[3]

	M_ODT_B0	AL26	SB_ODT[0]
	M_ODT_B1	AP26	SB_ODT[1]
	M_ODT_B2	AM26	SB_ODT[2]
	M_ODT_B3	AK26	SB_ODT[3]

[8]	M_DCLKB0	AL21	SB_CK[0]
[8]	M_DCLKB0	AL22	SB_CK[0]
[8]	M_DCLKB1	AL20	SB_CK[1]
[8]	M_DCLKB1	AK20	SB_CK[1]
[8]	M_DCLKB2	AL23	SB_CK[2]
[8]	M_DCLKB2	AM22	SB_CK[2]
[8]	M_DCLKB3	AP21	SB_CK[3]
[8]	M_DCLKB3	AN21	SB_CK[3]

[8]	M_VREF_DQB	AH1	FC_AH1
[8]	M_VREF_DQA	AH4	FC_AH4

[8]	M_VREF_DQB	AH1	FC_AH1
[8]	M_VREF_DQA	AH4	FC_AH4

	AU35	M_DA32	SA_DQ[32]
	AW37	M_DA33	SA_DQ[33]
	AU39	M_DA34	SA_DQ[34]
	AU36	M_DA35	SA_DQ[35]
	AY36	M_DA36	SA_DQ[36]
	AU37	M_DA37	SA_DQ[37]
	AU38	M_DA38	SA_DQ[38]
	AU37	M_DA39	SA_DQ[39]

	AP38	M_DQSA5	SA_DQS[5]
	AP39	M_DQSA5	SA_DQS[5]

	AR40	M_DA40	SA_DQ[40]
	AR37	M_DA41	SA_DQ[41]
	AN38	M_DA42	SA_DQ[42]
	AN37	M_DA43	SA_DQ[43]
	AR39	M_DA44	SA_DQ[44]
	AR38	M_DA45	SA_DQ[45]
	AN39	M_DA46	SA_DQ[46]
	AN40	M_DA47	SA_DQ[47]

	AK38	M_DQSA6	SA_DQS[6]
	AK39	M_DQSA6	SA_DQS[6]

	AL40	M_DA48	SA_DQ[48]
	AL37	M_DA49	SA_DQ[49]
	AJ38	M_DA50	SA_DQ[50]
	AJ37	M_DA51	SA_DQ[51]
	AL39	M_DA52	SA_DQ[52]
	AL38	M_DA53	SA_DQ[53]
	AJ39	M_DA54	SA_DQ[54]
	AJ40	M_DA55	SA_DQ[55]

	AF38	M_DQSA7	SA_DQS[7]
	AF39	M_DQSA7	SA_DQS[7]

	AG40	M_DA56	SA_DQ[56]
	AG37	M_DA57	SA_DQ[57]
	AE38	M_DA58	SA_DQ[58]
	AE37	M_DA59	SA_DQ[59]
	AG39	M_DA60	SA_DQ[60]
	AG38	M_DA61	SA_DQ[61]
	AE39	M_DA62	SA_DQ[62]
	AE40	M_DA63	SA_DQ[63]

[7] M\_ODT\_A[0..3] &lt; M\_ODT\_A[0..3]

[8] M\_ODT\_B[0..3] &lt; M\_ODT\_B[0..3]

[7] M\_DA[0..63] &lt; M\_DA[0..63]

[8] M\_DB[0..63] &lt; M\_DB[0..63]

[7] M\_DQSA[0..7] &lt; M\_DQSA[0..7]

[7] M\_DQSA[0..7] &lt; M\_DQSA[0..7]

[7] M\_AA[0..15] &lt; M\_AA[0..15]

[8] M\_AAB[0..15] &lt; M\_AAB[0..15]

[8] M\_DQSB[0..7] &lt; M\_DQSB[0..7]

[8] M\_DQSB[0..7] &lt; M\_DQSB[0..7]

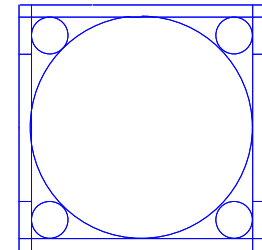
DDR\_1

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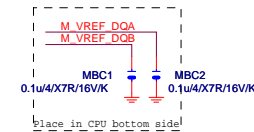
LGA1155[10SC1-F01155-01R]

LGA1155

ILM\_BP/1156/BKN/[12KRC-0F0001-23R]



Need check the new CPU ME



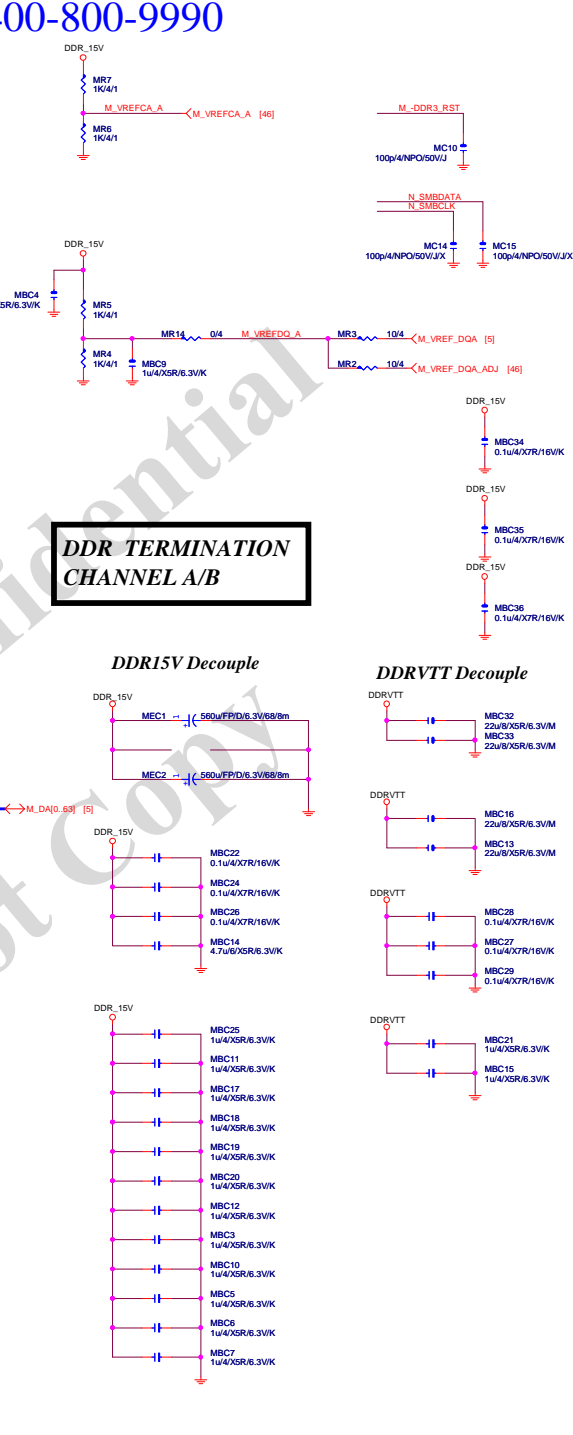
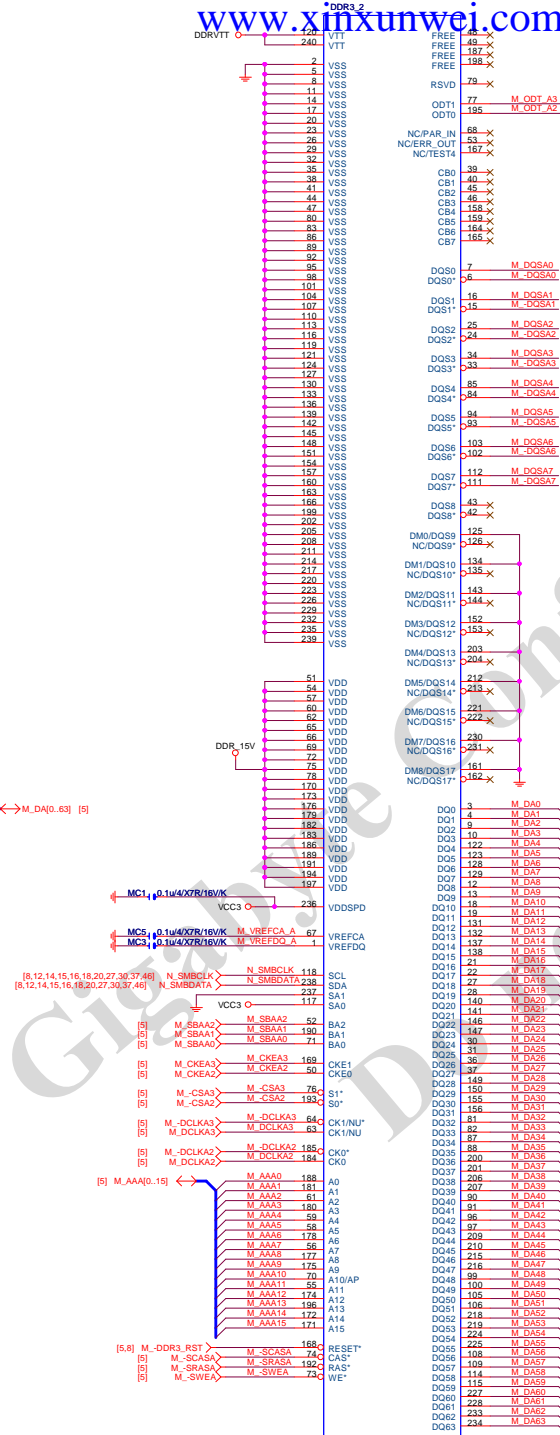
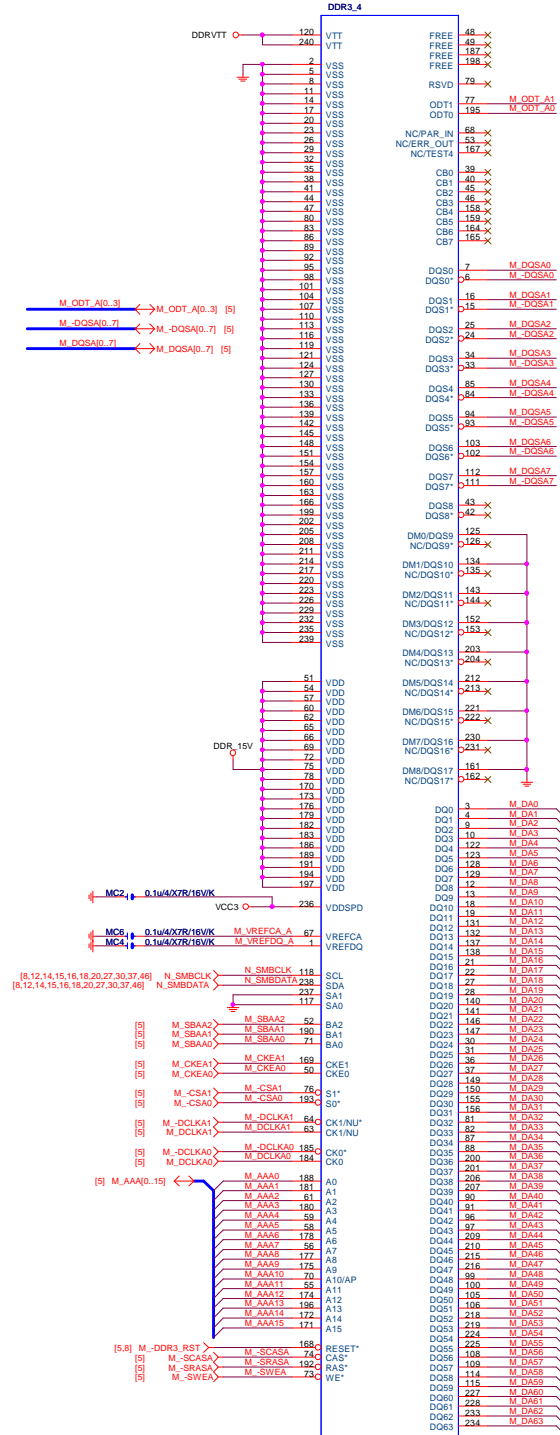
Gigabyte Technology

CPU LGA1156-B

Title	Document Number	Rev
	GA-Z77X-UD5H	1.1
Date:	Wednesday, June 06, 2012	Sheet 5 of 47

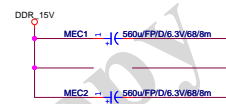




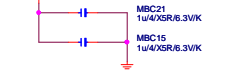
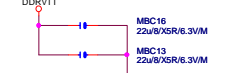
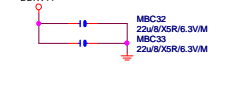


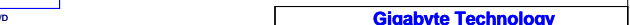
## DDR TERMINATION CHANNEL A/B

### DDR15V Decouple



### DDRVTT Decouple



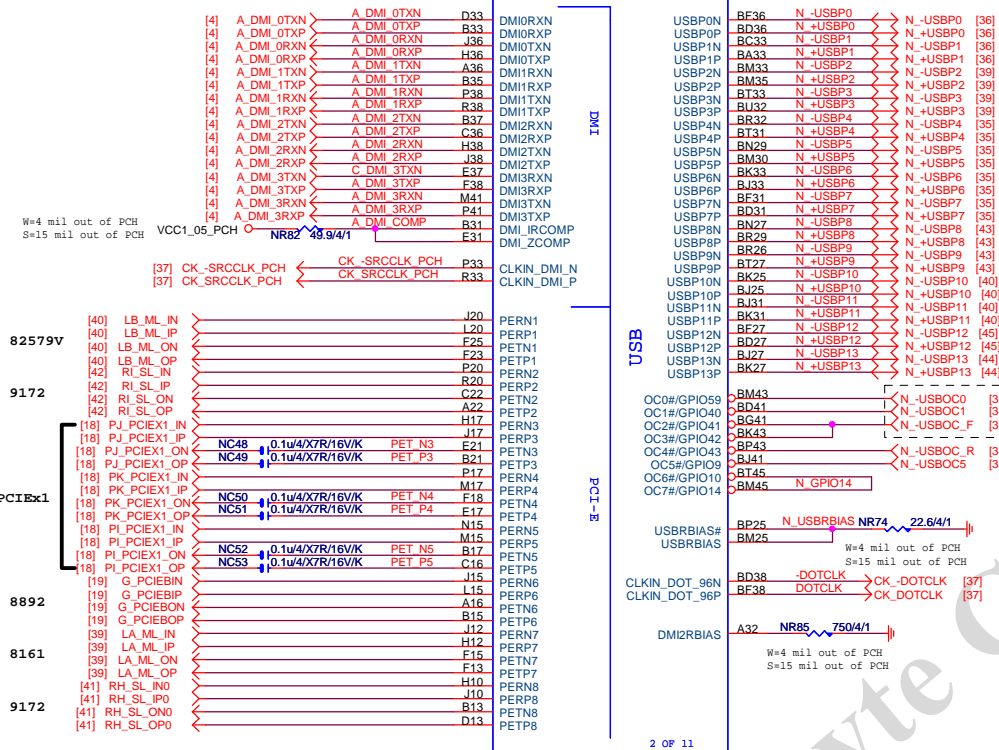




PCHB

USB:12/7.5/4.5/7.5/12 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%

PCHG



[45]

PCH\_USB3\_RXN3

&gt;

J25

PCH\_USB3\_RXP3

&gt;

J25

PCH\_USB3\_TXN3

&gt;

J25

PCH\_USB3\_TXP3

&gt;

J25

NBC90

0.1u/4/X7R/16V/K

J25

NBC91

0.1u/4/X7R/16V/K

J25

J22

PCH\_USB3\_RXN4

&gt;

J22

PCH\_USB3\_RXP4

&gt;

J22

PCH\_USB3\_TXN4

&gt;

J22

PCH\_USB3\_TXP4

&gt;

J22

NBC92

0.1u/4/X7R/16V/K

J22

NBC93

0.1u/4/X7R/16V/K

J22

J22

PCH\_USB3\_RXN4

&gt;

J22

PCH\_USB3\_RXP4

&gt;

J22

PCH\_USB3\_TXN4

&gt;

J22

PCH\_USB3\_TXP4

&gt;

J22

OC[3:0]# for

Device 29

(ports 0-7)

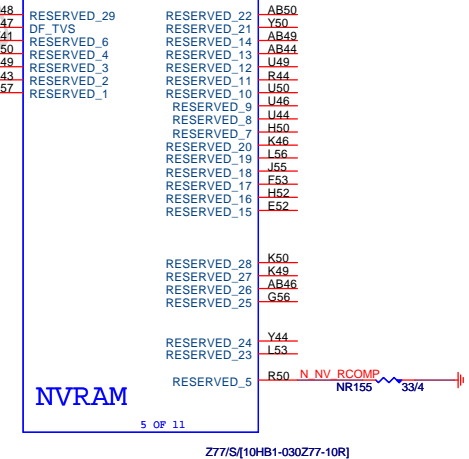
OC[7:4]# for

Device 26

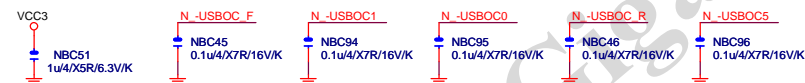
(ports 8-13)

USB OC# Configure	
OC0#	F_USB30_1
OC1#	USB30_LAN1
OC2#	F_USB1
OC3#	F_USB2
OC4#	ESATA_1394_USB
OC5#	USB30_LAN2
OC6#	Not Use
OC7#	Not Use

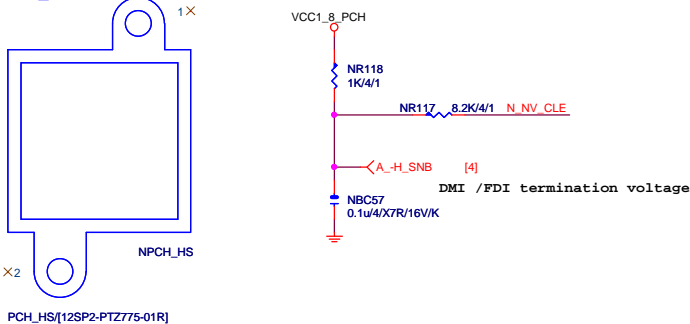
PCHC

PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)  
Impedance=80 +- 17.5%

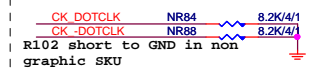
Z77/S[10HB1-030Z77-10R]



PCH\_HS

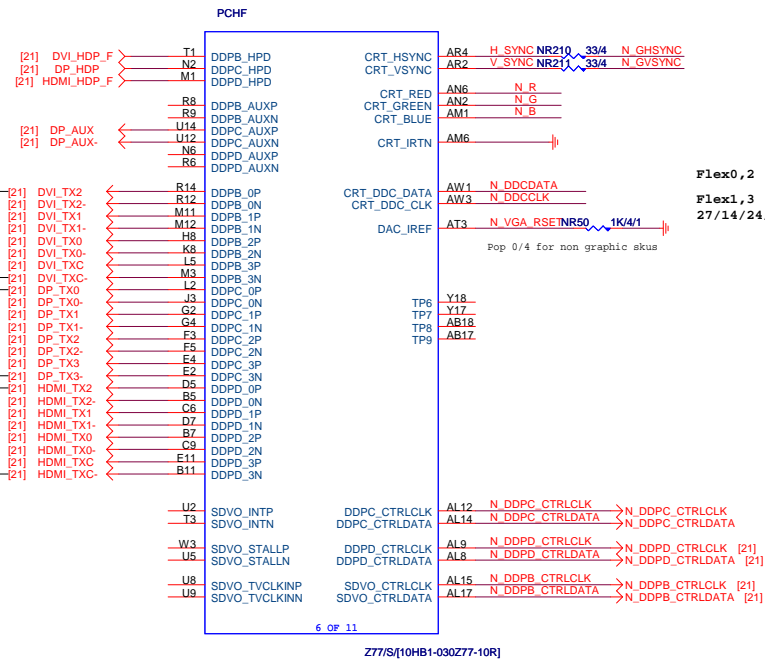


Mount for integrated clock Generation Mode

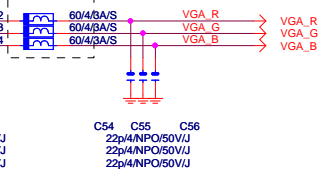
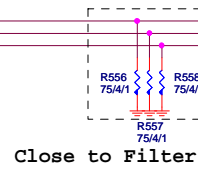
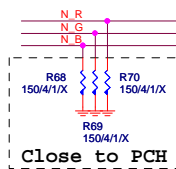
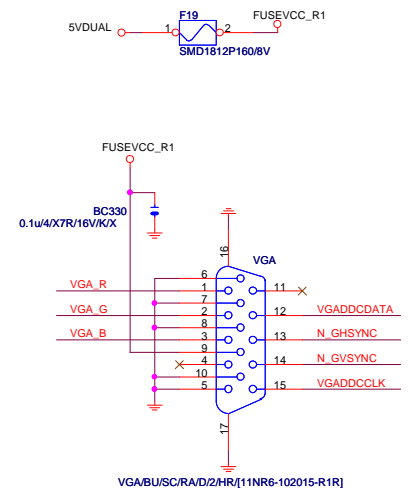
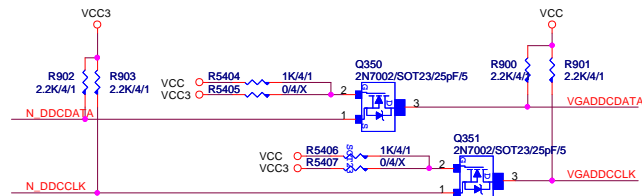
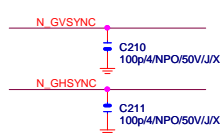
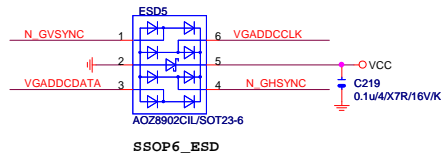
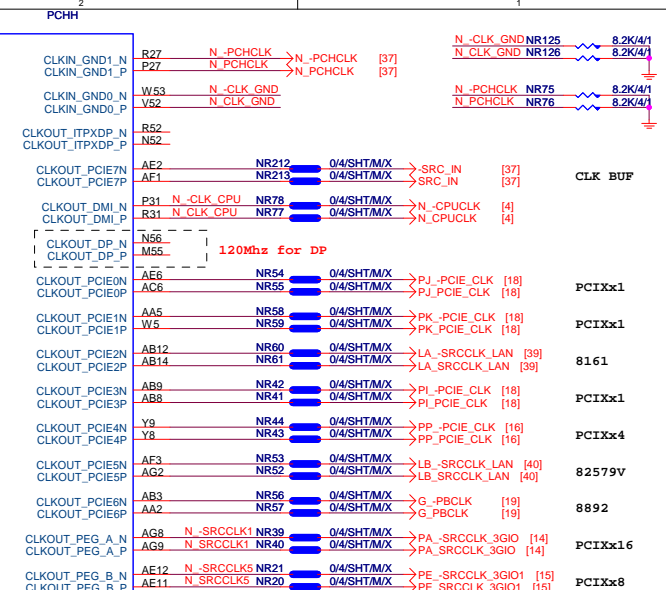
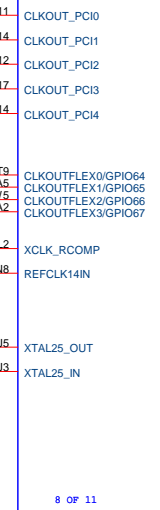
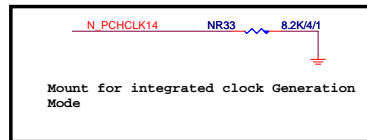
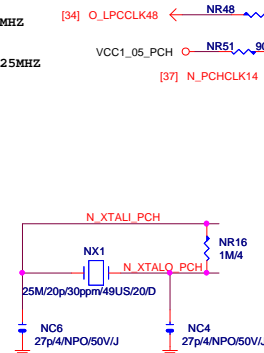


## Gigabyte Technology

Title		PCH FDI,DMI,USB ,PCIE	
Size	Document Number	GA-Z77X-UD5H	
Custom		Rev 1.1	
Date:	Tuesday, June 19, 2012	Sheet 9	of 47



Flex0,2 : 33MHz  
Flex1,3 : 27/14/24/48/25MHz



SATA:20/7.5/4.5/7.5/20 (breakout min 8/4/4/8)  
Impedance=90 +- 17.5%

PCHC

For WIFI  
BA50  
BF50  
BF49

CL\_CLK1  
CL\_DATA1  
CL\_RST1#

APWROK  
PWM0  
PWM1  
PWM2  
PWM3

BT17  
BT21  
BT20  
BT19

TACH0/GPIO17  
TACH1/GPIO1  
TACH2/GPIO6  
TACH3/GPIO7

TACH4\_GPIO68  
TACH5\_GPIO69  
TACH6\_GPIO70  
TACH7\_GPIO71

SST  
SSTCTL

SCLOCK/GPIO22  
SLOAD/GPIO38  
SDATAOUT0/GPIO39  
SDATAOUT1/GPIO48

NC\_5  
AY20

NC19  
0.01u/4/X7R/25V/K/X

N\_GPIO17  
N\_GPIO1  
N\_GPIO6  
N\_GPIO68  
N\_GPIO69  
N\_GPIO70  
N\_GPIO71

N\_GPIO22  
N\_GPIO38  
N\_GPIO39  
N\_GPIO48

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N\_GPIO68

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SATA0GP

SATA0GP

SATA3

SATA2

SATA1

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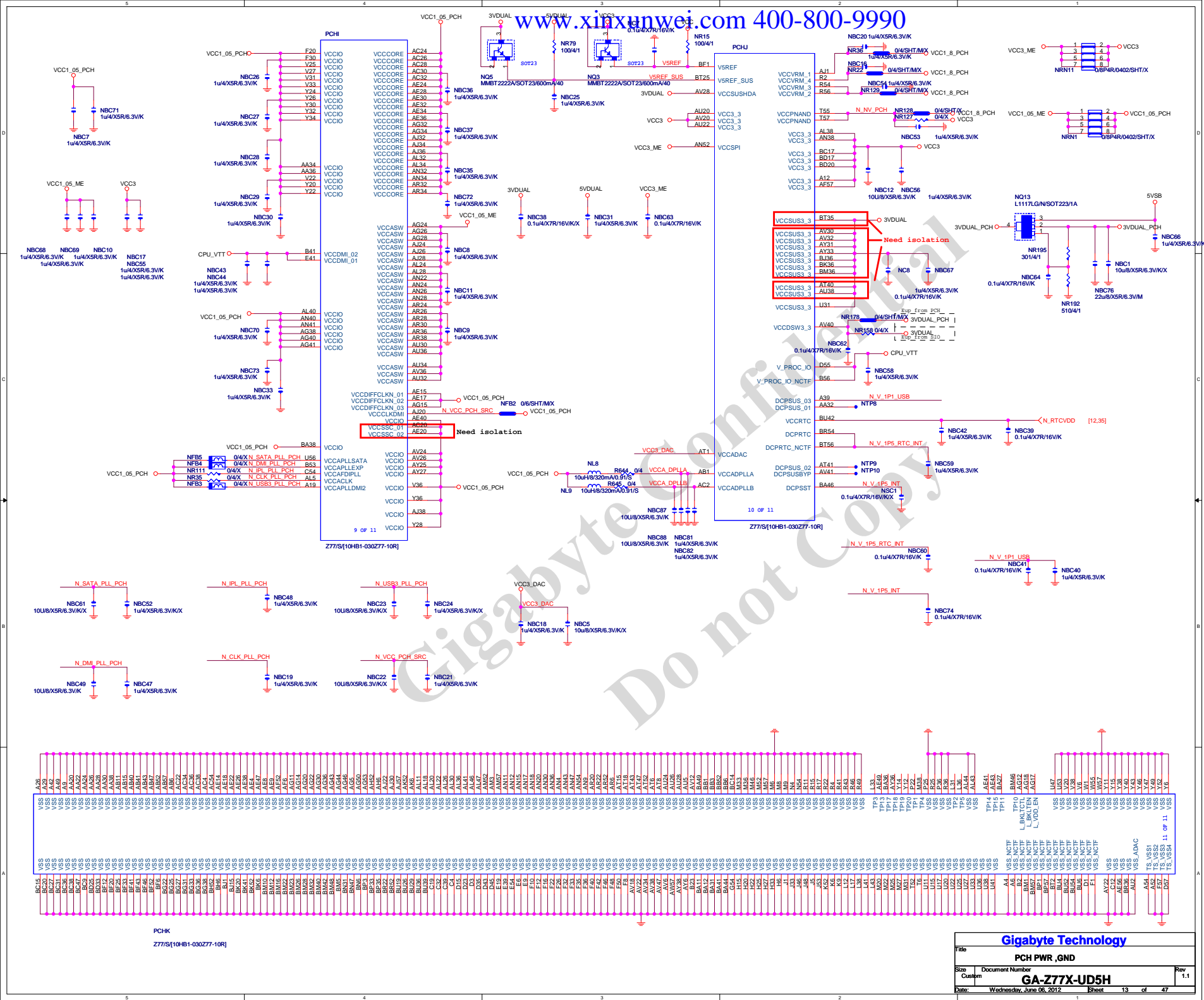
SATA0GP

SATA0GP

SATA0GP

SATA0GP







**+12 protect  
short-wire test**

PCIEX16:16/5/5/16

PA\_EXP\_RXP[0..15] >> PA\_EXP\_RXP[0..15] [4,17]  
PA\_EXP\_RXN[0..15] >> PA\_EXP\_RXN[0..15] [4,17]  
PA\_EXP\_TXP[0..15] >> PA\_EXP\_TXP[0..15] [4,17]  
PA\_EXP\_TXN[0..15] >> PA\_EXP\_TXN[0..15] [4,17]

PA_EXP_TXP0	PAC5	0.22u/4/X5R6.3V/K	PA_EXP_TXP0_C
PA_EXP_TXN0	PAC4	0.22u/4/X5R6.3V/K	PA_EXP_TXN0_C
PA_EXP_TXP1	PAC6	0.22u/4/X5R6.3V/K	PA_EXP_TXP1_C
PA_EXP_TXN1	PAC7	0.22u/4/X5R6.3V/K	PA_EXP_TXN1_C
PA_EXP_TXP2	PAC8	0.22u/4/X5R6.3V/K	PA_EXP_TXP2_C
PA_EXP_TXN2	PAC9	0.22u/4/X5R6.3V/K	PA_EXP_TXN2_C
PA_EXP_TXP3	PAC10	0.22u/4/X5R6.3V/K	PA_EXP_TXP3_C
PA_EXP_TXN3	PAC11	0.22u/4/X5R6.3V/K	PA_EXP_TXN3_C
PA_EXP_TXP4	PAC12	0.22u/4/X5R6.3V/K	PA_EXP_TXP4_C
PA_EXP_TXN4	PAC13	0.22u/4/X5R6.3V/K	PA_EXP_TXN4_C
PA_EXP_TXP5	PAC14	0.22u/4/X5R6.3V/K	PA_EXP_TXP5_C
PA_EXP_TXN5	PAC15	0.22u/4/X5R6.3V/K	PA_EXP_TXN5_C
PA_EXP_TXP6	PAC16	0.22u/4/X5R6.3V/K	PA_EXP_TXP6_C
PA_EXP_TXN6	PAC17	0.22u/4/X5R6.3V/K	PA_EXP_TXN6_C
PA_EXP_TXP7	PAC18	0.22u/4/X5R6.3V/K	PA_EXP_TXP7_C
PA_EXP_TXN7	PAC19	0.22u/4/X5R6.3V/K	PA_EXP_TXN7_C
PA_EXP_SW_TXP8	PAC20	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP8_C
PA_EXP_SW_TXN8	PAC21	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN8_C
PA_EXP_SW_TXP9	PAC22	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP9_C
PA_EXP_SW_TXN9	PAC23	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN9_C
PA_EXP_SW_TXP10	PAC24	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP10_C
PA_EXP_SW_TXN10	PAC25	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN10_C
PA_EXP_SW_TXP11	PAC26	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP11_C
PA_EXP_SW_TXN11	PAC27	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN11_C
PA_EXP_SW_TXP12	PAC28	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP12_C
PA_EXP_SW_TXN12	PAC29	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN12_C
PA_EXP_SW_TXP13	PAC30	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP13_C
PA_EXP_SW_TXN13	PAC31	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN13_C
PA_EXP_SW_TXP14	PAC32	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP14_C
PA_EXP_SW_TXN14	PAC33	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN14_C
PA_EXP_SW_TXP15	PAC34	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP15_C
PA_EXP_SW_TXN15	PAC35	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN15_C

PA\_EXP\_SW\_RXP[8..15] >> PA\_EXP\_SW\_RXP[8..15] [17]  
PA\_EXP\_SW\_RXN[8..15] >> PA\_EXP\_SW\_RXN[8..15] [17]  
PA\_EXP\_SW\_TXP[8..15] >> PA\_EXP\_SW\_TXP[8..15] [17]  
PA\_EXP\_SW\_TXN[8..15] >> PA\_EXP\_SW\_TXN[8..15] [17]

PCI-E REV:1.1--> 2.5GHZ

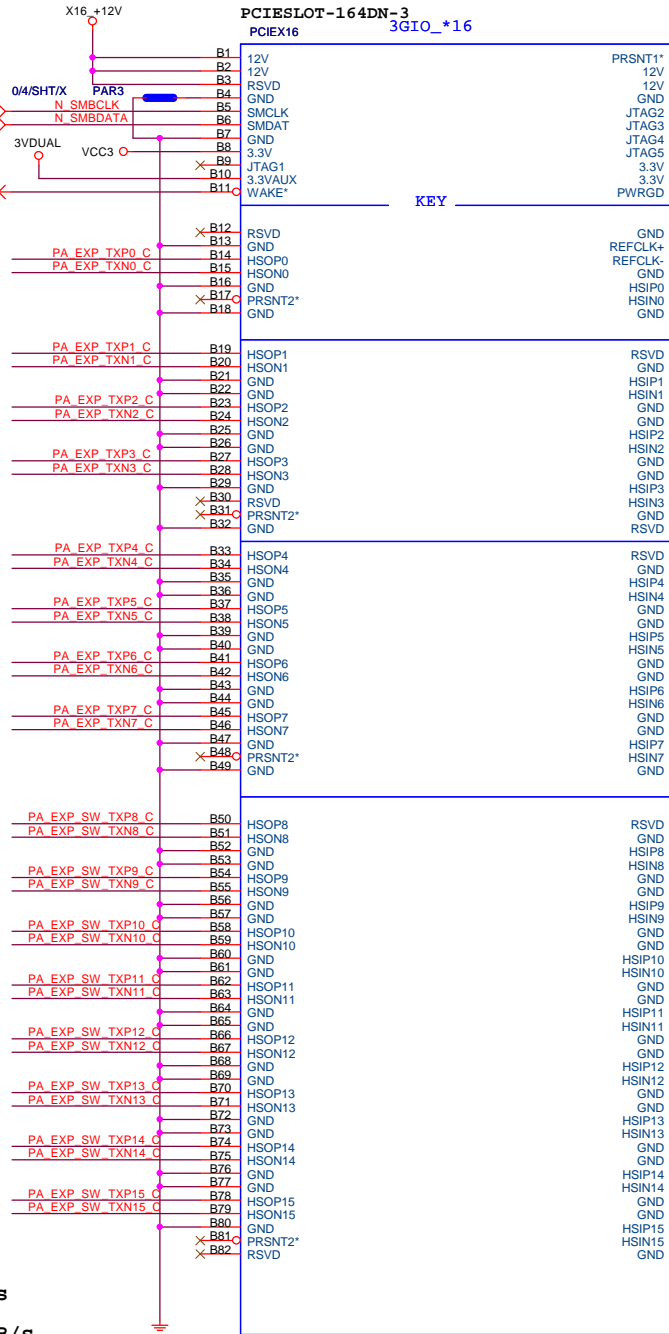
PCE-E X1(單向) BANDWITH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

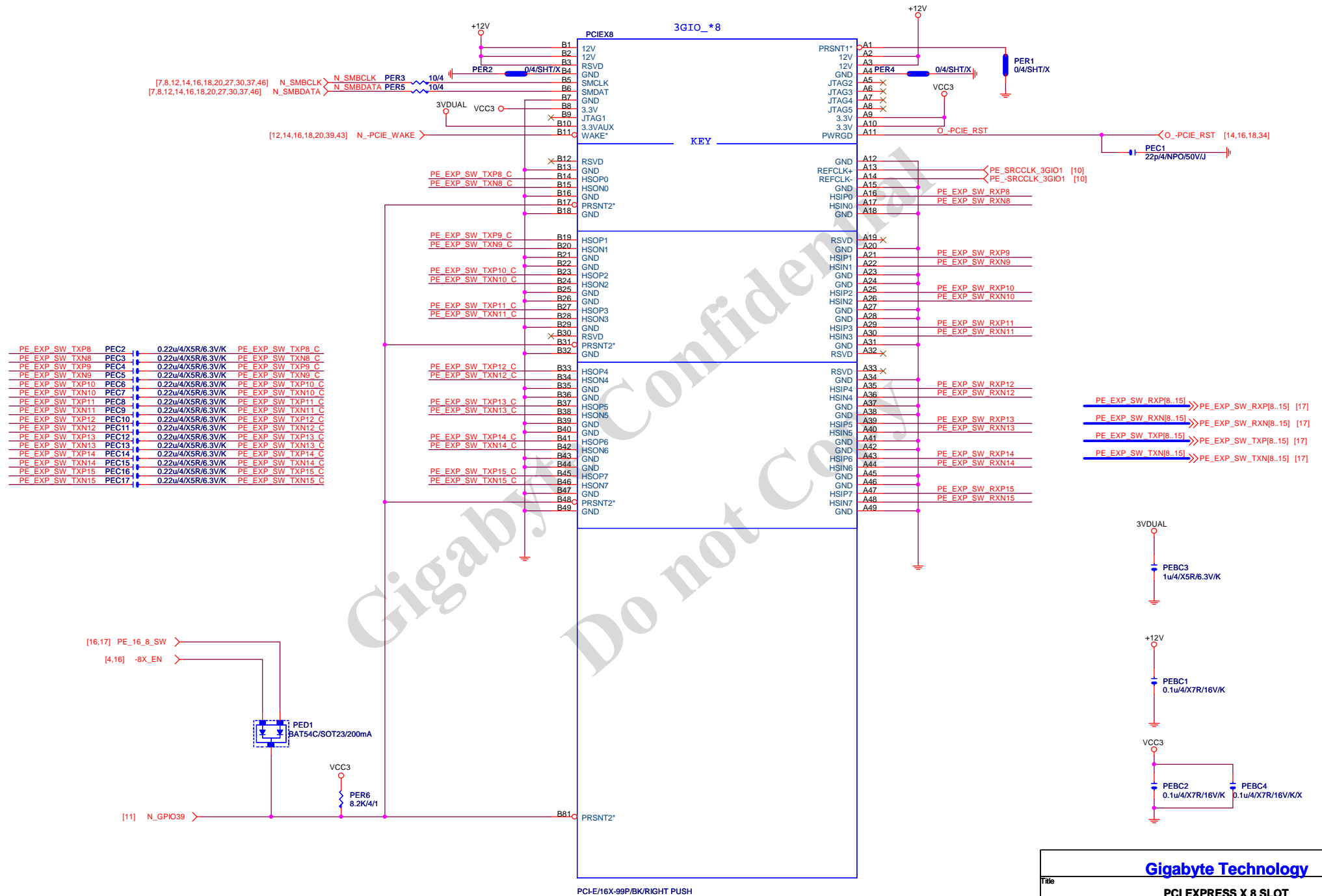


PCI-E/16X-164P/BK/RIGHT PUSH

**Gigabyte Technology**

Title		PCI EXPRESS * 16 SLOT	
Size	Document Number	GA-Z77X-UD5H	
Custom		Rev 1.1	
Date:	Wednesday, June 06, 2012	Sheet	14 of 47



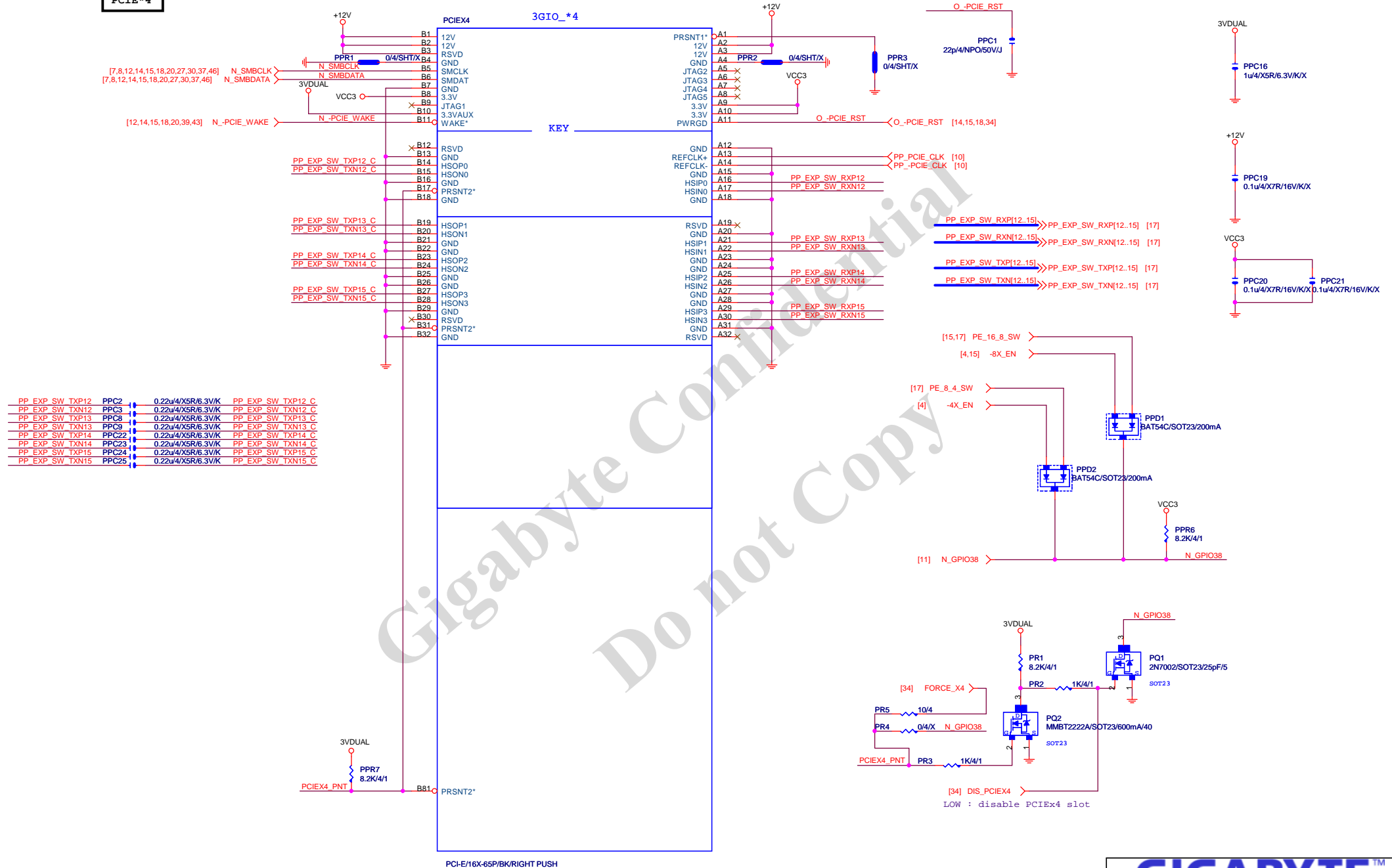


PCI-E/16X-99P/BK/RIGHT PUSH

Gigabyte Technology

Title		PCI EXPRESS X 8 SLOT	
Size	Document Number	GA-Z77X-UD5H	
Custom		Rev 1.1	
Date:	Tuesday, June 19, 2012	Sheet	15 of 47

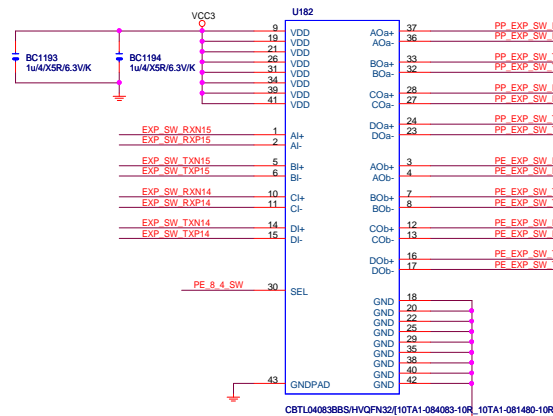
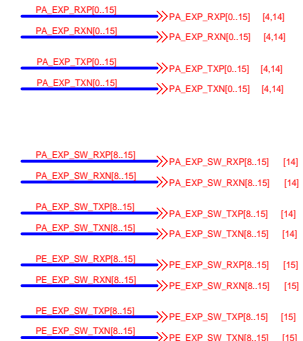
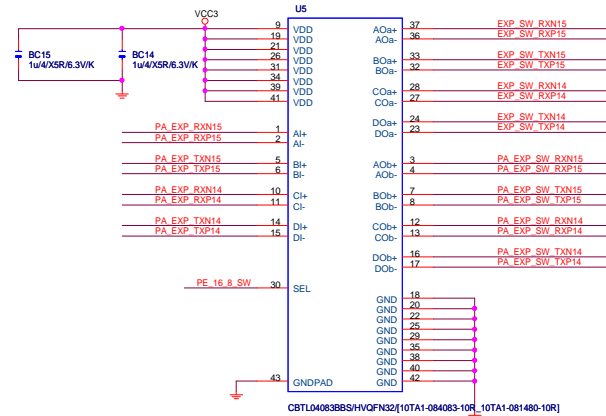
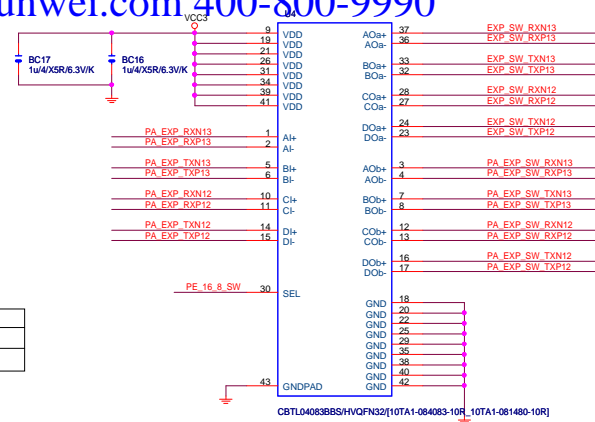
PCIE\*4



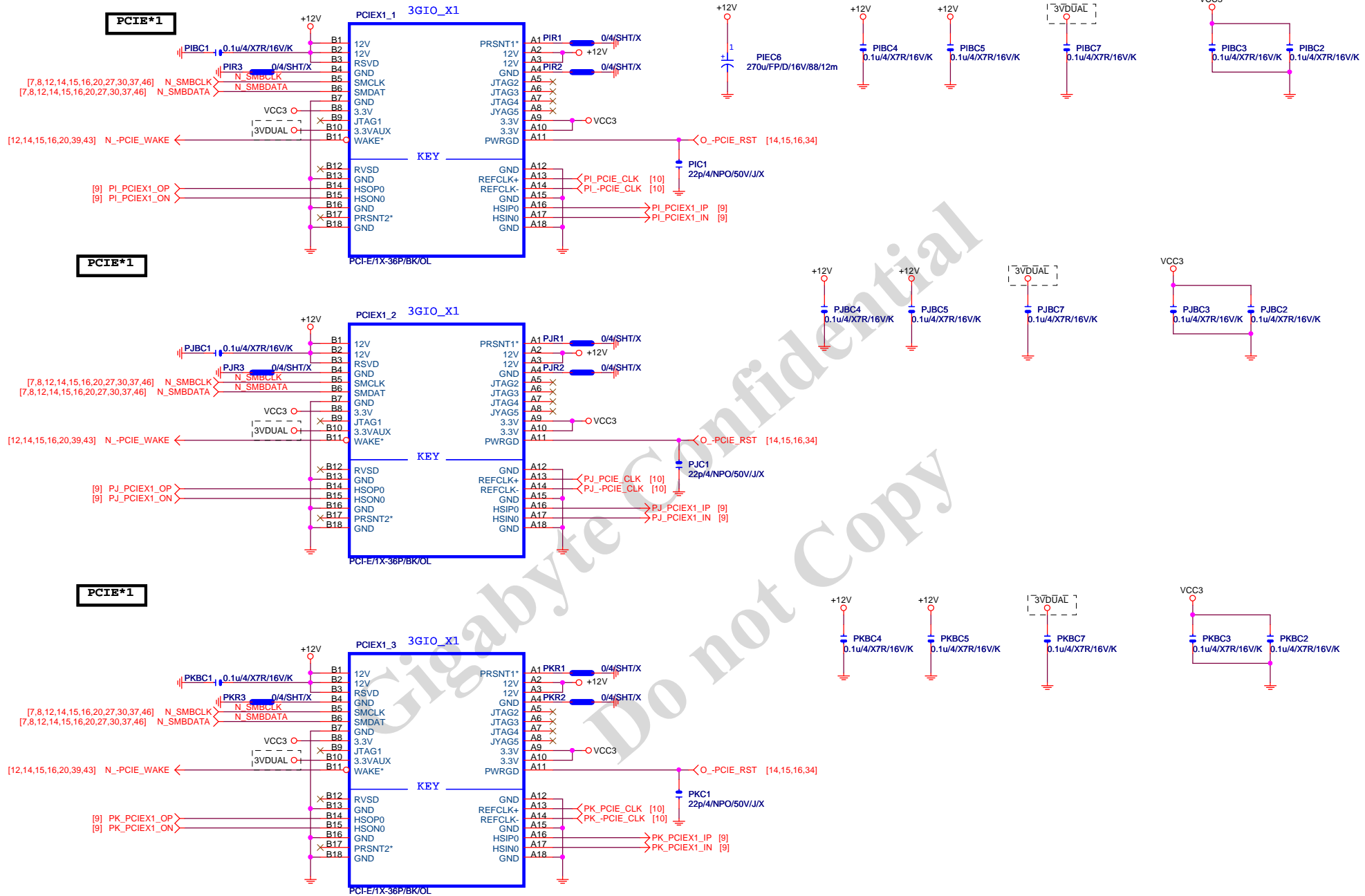
PCI-E/16X-65P/BK/RIGHT PUSH

# GIGABYTE™

Title <b>PCI EXPRESS X4 SLOT</b>		
Size Custom	Document Number <b>GA-Z77X-UD5H</b>	Rev <b>1.1</b>
Date: Wednesday, June 06, 2012	Sheet 16	of 47



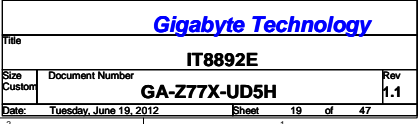
Function	SEL
xI--> x0a	L
xI--> x0b	H



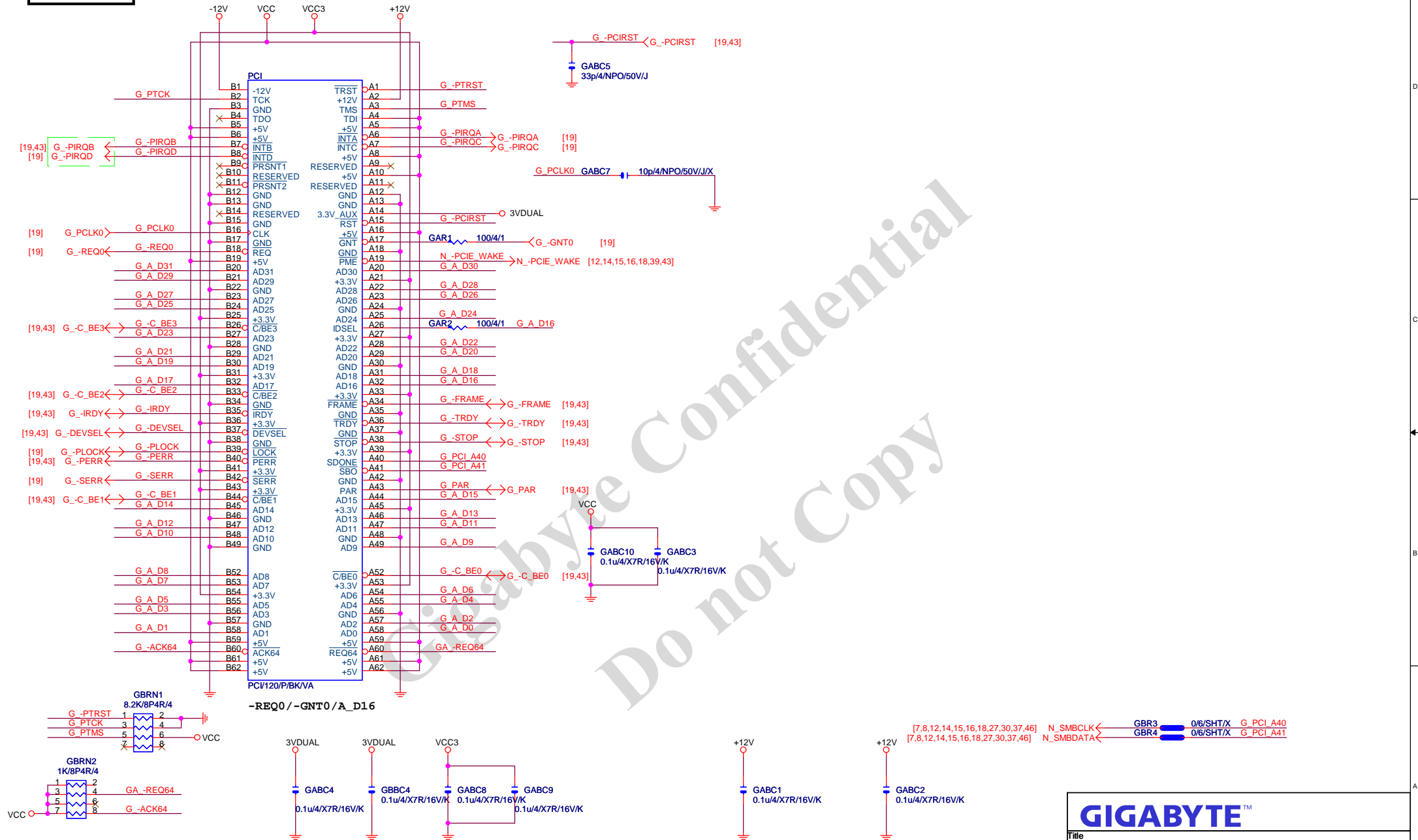
Gigabyte Technology

Title			PCIEX1_1, 2, 3
Size	Document Number		
Custom		GA-Z77X-UD5H	
Date:	Wednesday, June 06, 2012	Sheet	18 of 47

Rev 1.1

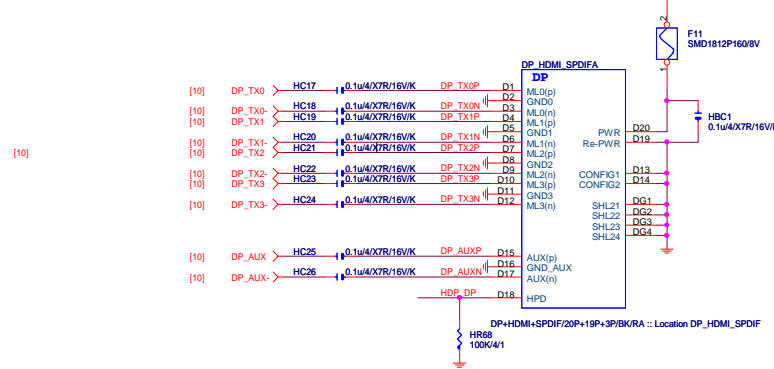
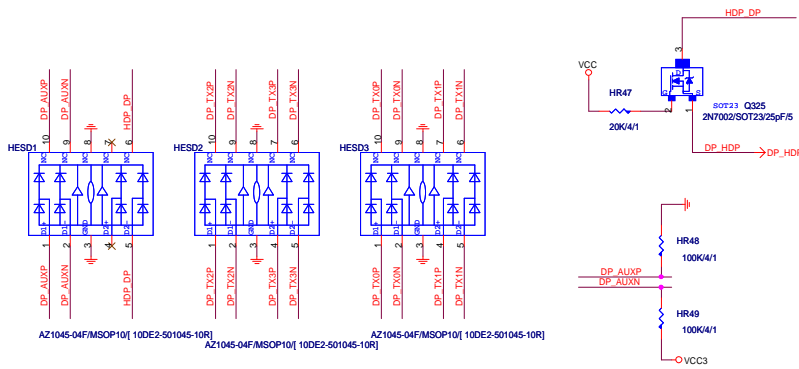
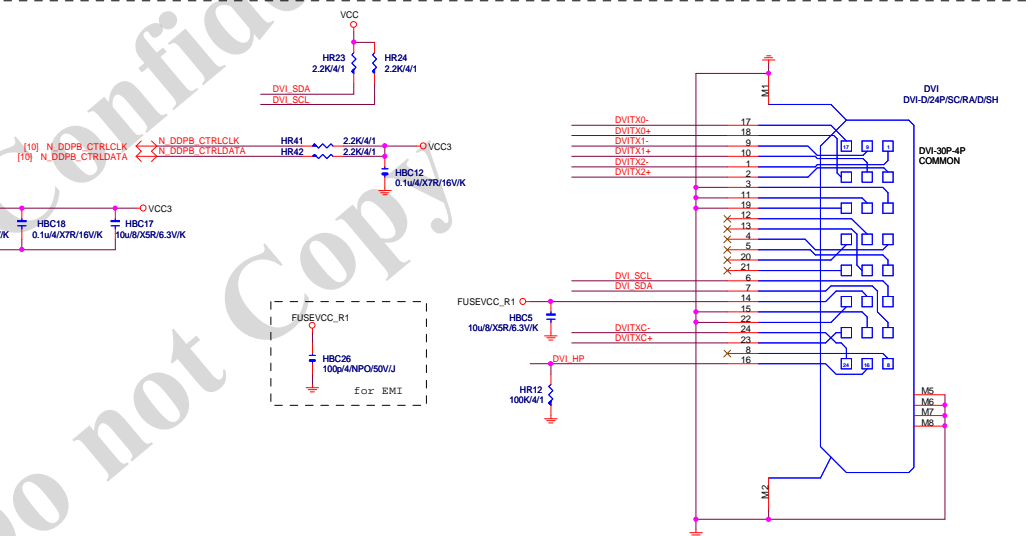
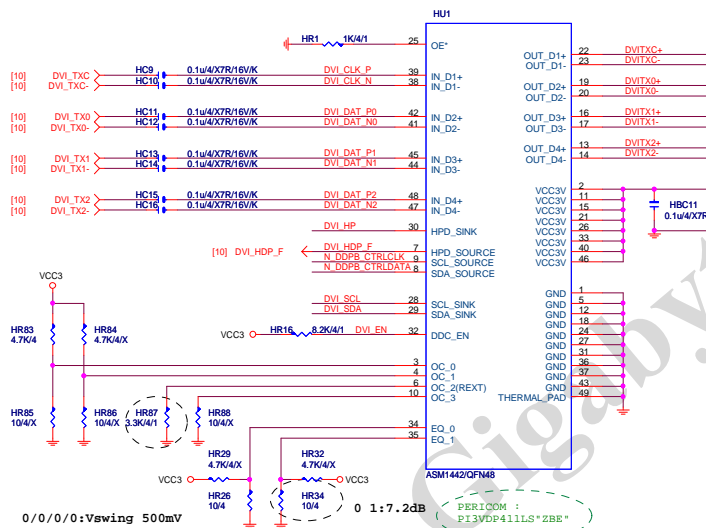
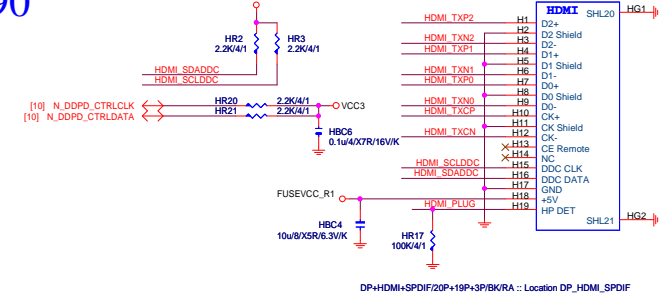
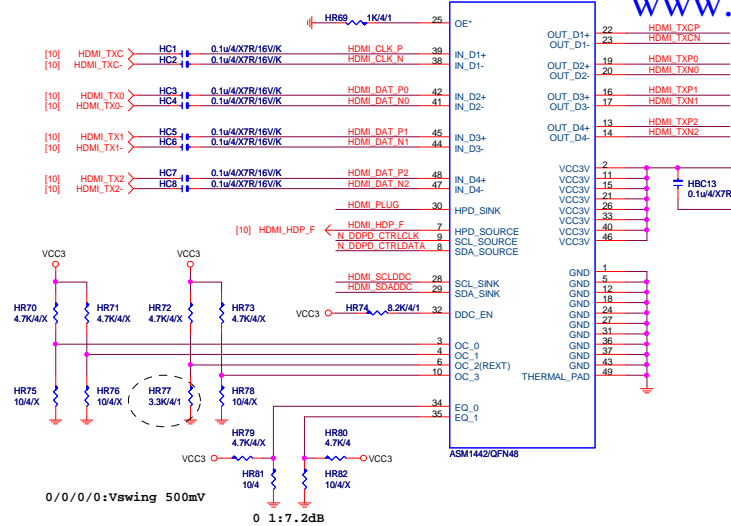


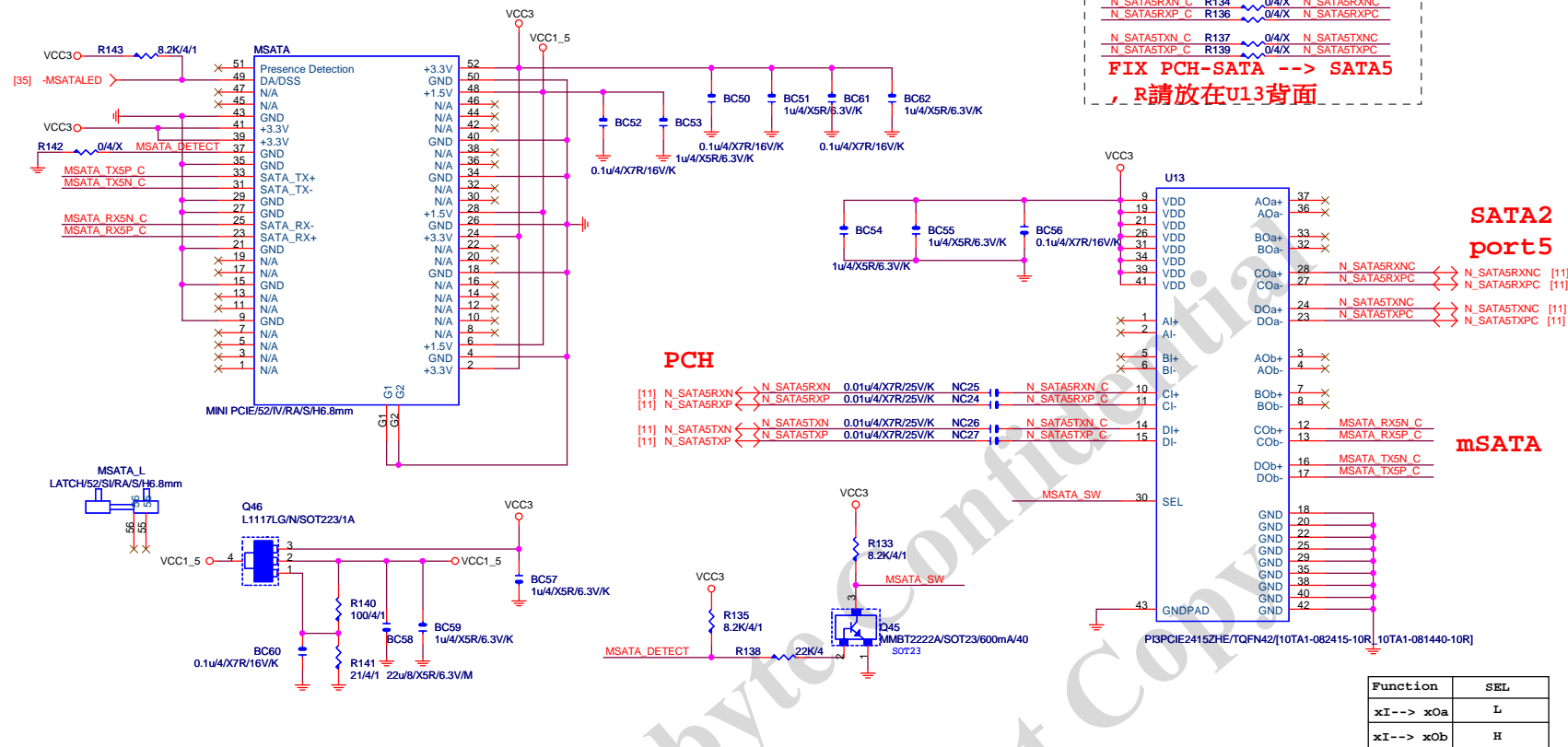
## PCI SLOT 1

**GIGABYTE™**

Title <b>PCI SLOT 1</b>		
Size Custom	Document Number <b>GA-Z77X-UD5H</b>	Rev <b>1.1</b>
Date: Wednesday, June 06, 2012 Sheet 20 of 47		







## MOSI For DMI RX Termination Voltage

[12] N\_ICH\_SPI\_MOSI >> ICH\_SPI\_MOSI NR10 8.2K/4/1/X  
 [12] N\_ICH\_SPI\_CS >> ICH\_SPI\_CS NR9 8.2K/4/1/X  
 [12] N\_ICH\_SPI\_CS >> SPI\_HOLD0 NR3 8.2K/4/1/X  
 [12] N\_ICH\_SPI\_MISO >> ICH\_SPI\_MISO NR5 8.2K/4/1/X

[12] N\_SPI\_WP1 >> SPI\_WP1 NR2 8.2K/4/1/X  
 [12] N\_SPI\_WP0 >> SPI\_WP0 NR1 8.2K/4/1/X  
 [12] N\_ICH\_SPI\_MISO >> ICH\_SPI\_MISO NR5 8.2K/4/1/X

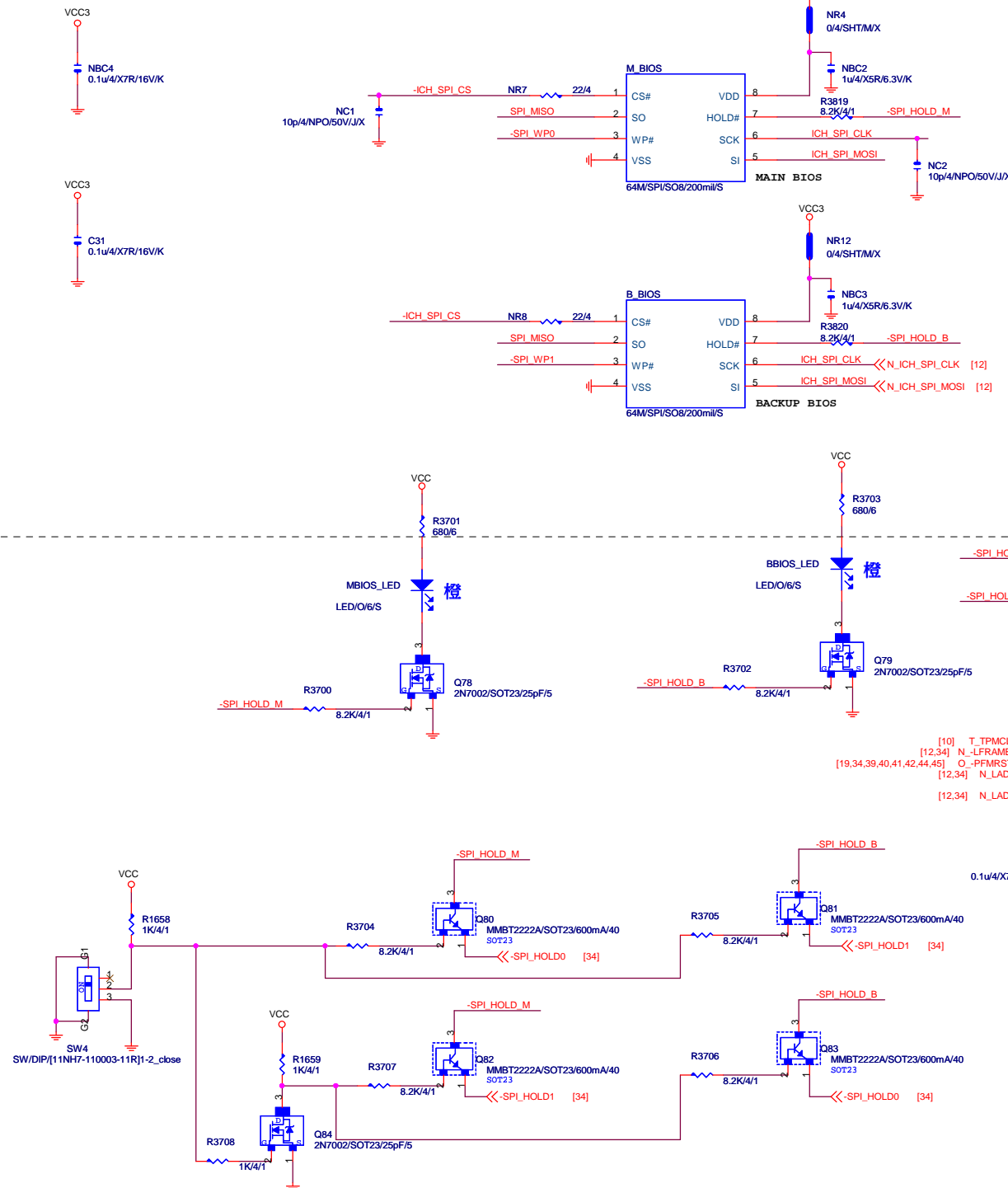
[11] N\_GNT0 >> NR26 1K/4/1/X  
 [11] N\_GNT1 >> NR25 1K/4/1/X

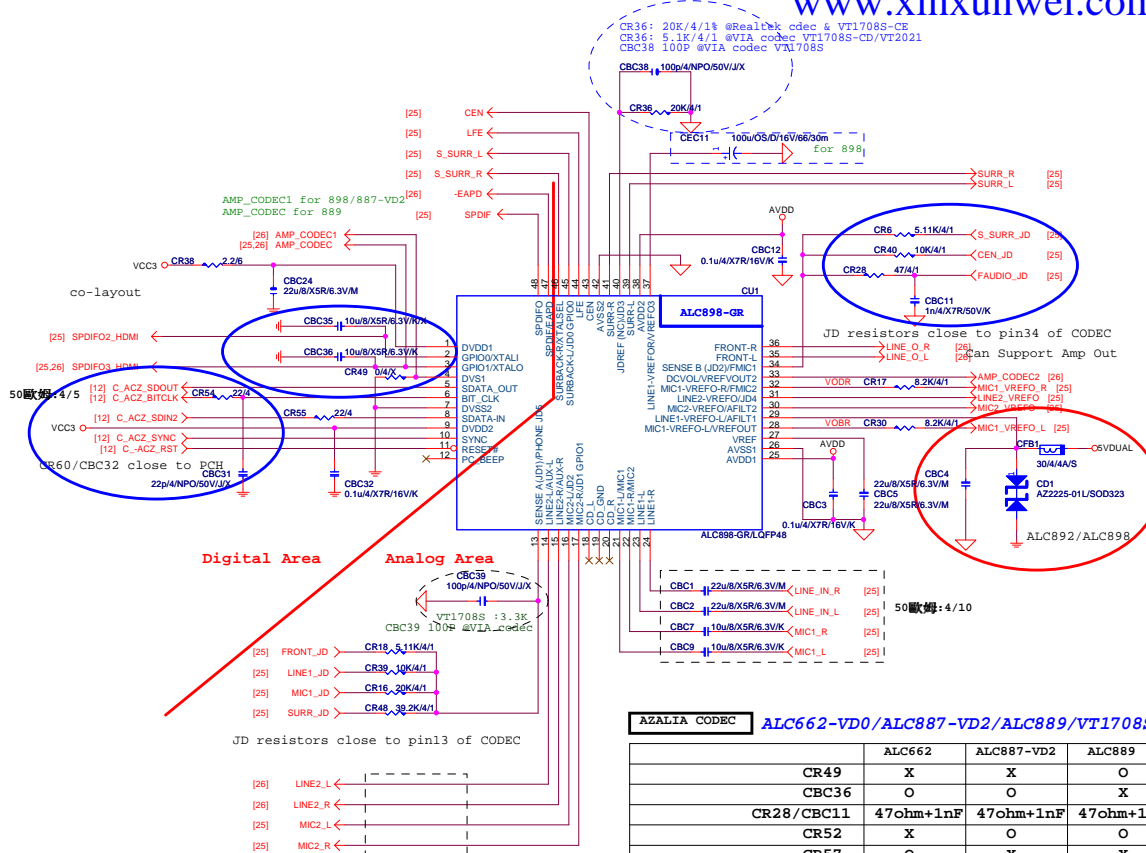
## Default int pull up

SPI\_MISO NR6 22/4 << N\_ICH\_SPI\_MISO [12]

BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

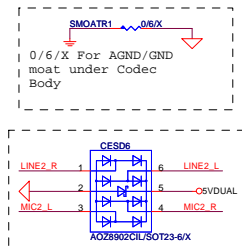
1 means floating  
0 means PD 1K



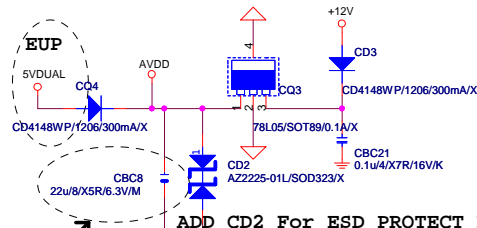


ALC889	ALC889B	ALC892	ALC898	Colay
CR49	O	O	X	
CBC36	X	X	10uF/X5R	
CBC35	X	10uF/X5R	X	
CR52	O	X	O	
CR53	X	O	X	
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	
CBC7/CBC9/CBC20/CBC15	10uF/X5R	10uF/X5R	10uF/X5R	
CFB1/CD1/CBC4	X	X	O	
CD2/CD3/CQ3/CQ4	O	O	X	
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47/ CR2/CR11/CR14/CR24	62 ohm	62 ohm	62 ohm	

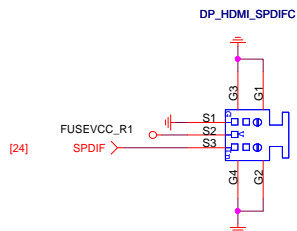
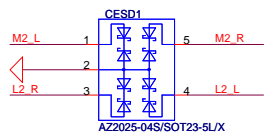
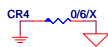
ALZALIA CODEC	ALC662-VD0/ALC887-VD2/ALC889/VT1708S-CD/VT1708S-CE/VT2021 Colay						
	ALC662	ALC887-VD2	ALC889	VT1708S-CD	VT1708S-CE	VT2021	ALC898/ALC899
CR49	X	X	O	O	X	O	X
CBC36	O	O	X	X	O	X	O
CR28/CBC11	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P	47ohm+1nF	47ohm+1nF
CR52	X	O	O	O	O	O	O
CR57	O	X	X	X	X	X	X
CBC1/CBC2	10uF/X5R	10uF/X5R	22uF/X5R	10uF/X5R	10uF/X5R	10uF/X5R	22uF/X5R
CR36	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1	5.1K/4/1	20K/4/1
CR17/CR30/ CR25/CR15/CR12/CR3/	8.2K/4	8.2K/4	8.2K/4	3.3K/4/1	3.3K/4/1	3.3K/4/1	8.2K/4
CBC38/CBC39	X	X	X	100P/4	100P/4	X	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR27/CR26	22K/4	22K/4	22K/4	10K/4/1	10K/4/1	10K/4/1	22K/4
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR2/CR11/ CR14/CR24	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm	75 ohm	62 ohm
CFB1/CD1/CBC4/CBC8	O	O	X	X	O	X	O
CD2/CD3/CQ3/CQ4	X	X	O	O	X	O	X
CEC11	X	X	X	X	X	X	O
CESD6	X	X	X	O	O	O	X



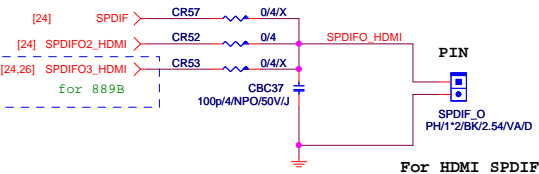
## CODEC POWER/EMI PAD



上ALC892時,此顆電容要保留

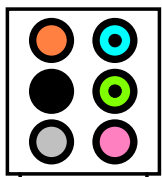


DP+HDMI+SPDIF/20P+19P+3P/BK/RA:: Location DP\_HDMI\_SPDIF

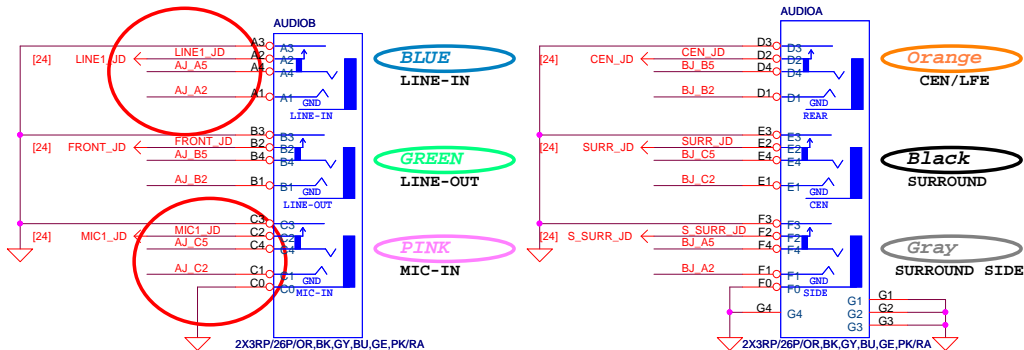
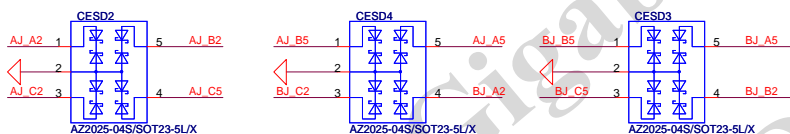


## AZALIA JACK

BTX AZALIA CONNECTOR



11NR6-403007-21R



Near Audio jack left

Codec --&gt; Audio jack

F\_AUDIO

LINE-IN

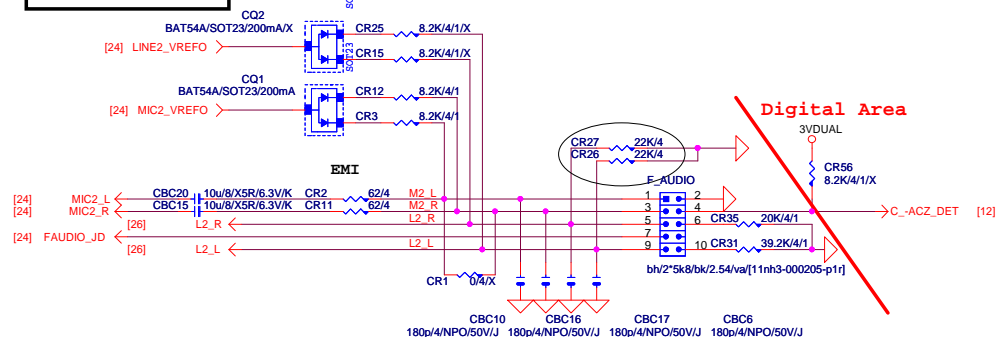
MIC-IN

SURROUND

CEN/LFE

SURR BACK

AZALIA FRONT PANEL

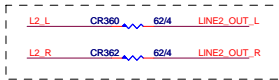
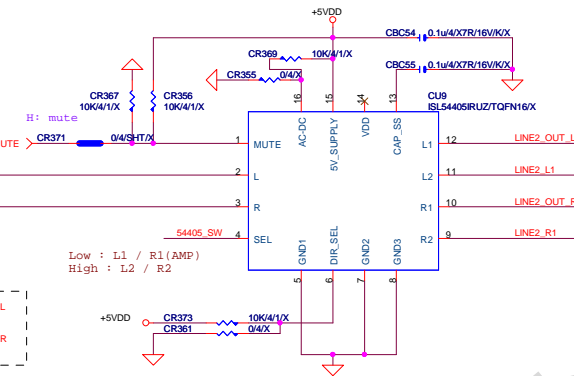
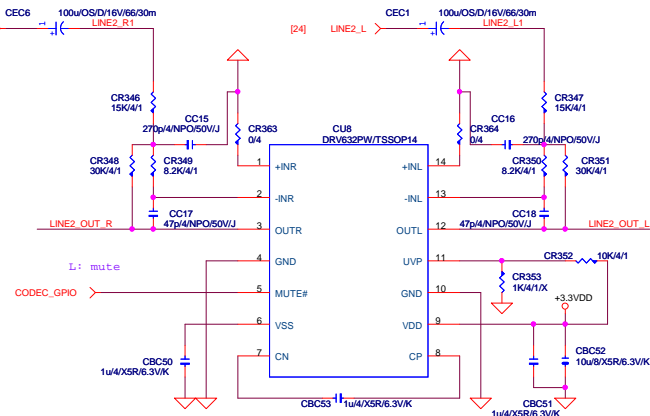


Digital Area

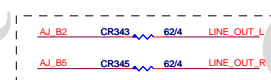
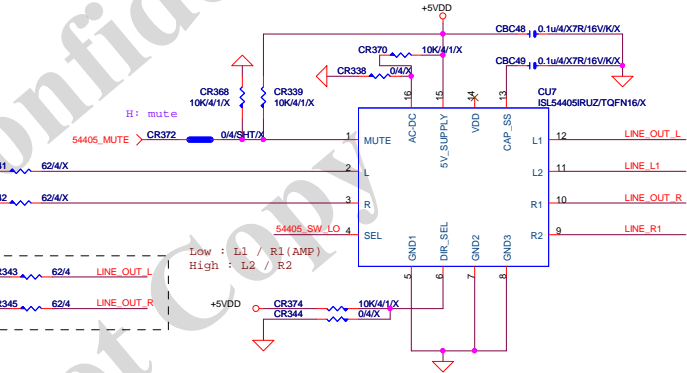
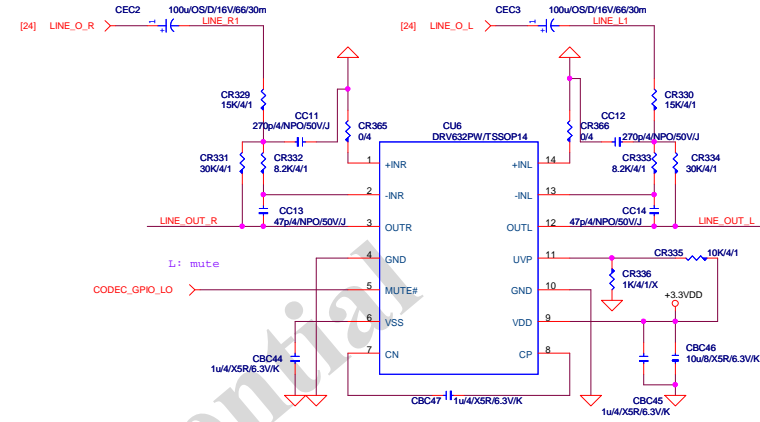
Gigabyte Technology

Title					AUDIO JACK						
Size	Custom	Document Number				GA-Z77X-UD5H				Rev	
										1.1	
Date:		Wednesday, June 06, 2012				Sheet		25		of 47	

## HEADPHONE



## LINE-OUT

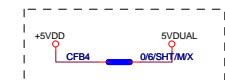
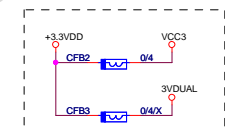
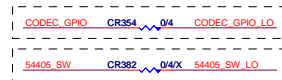
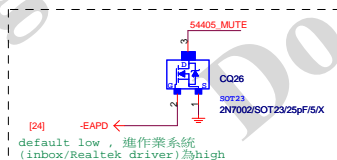


## HEADPHONE

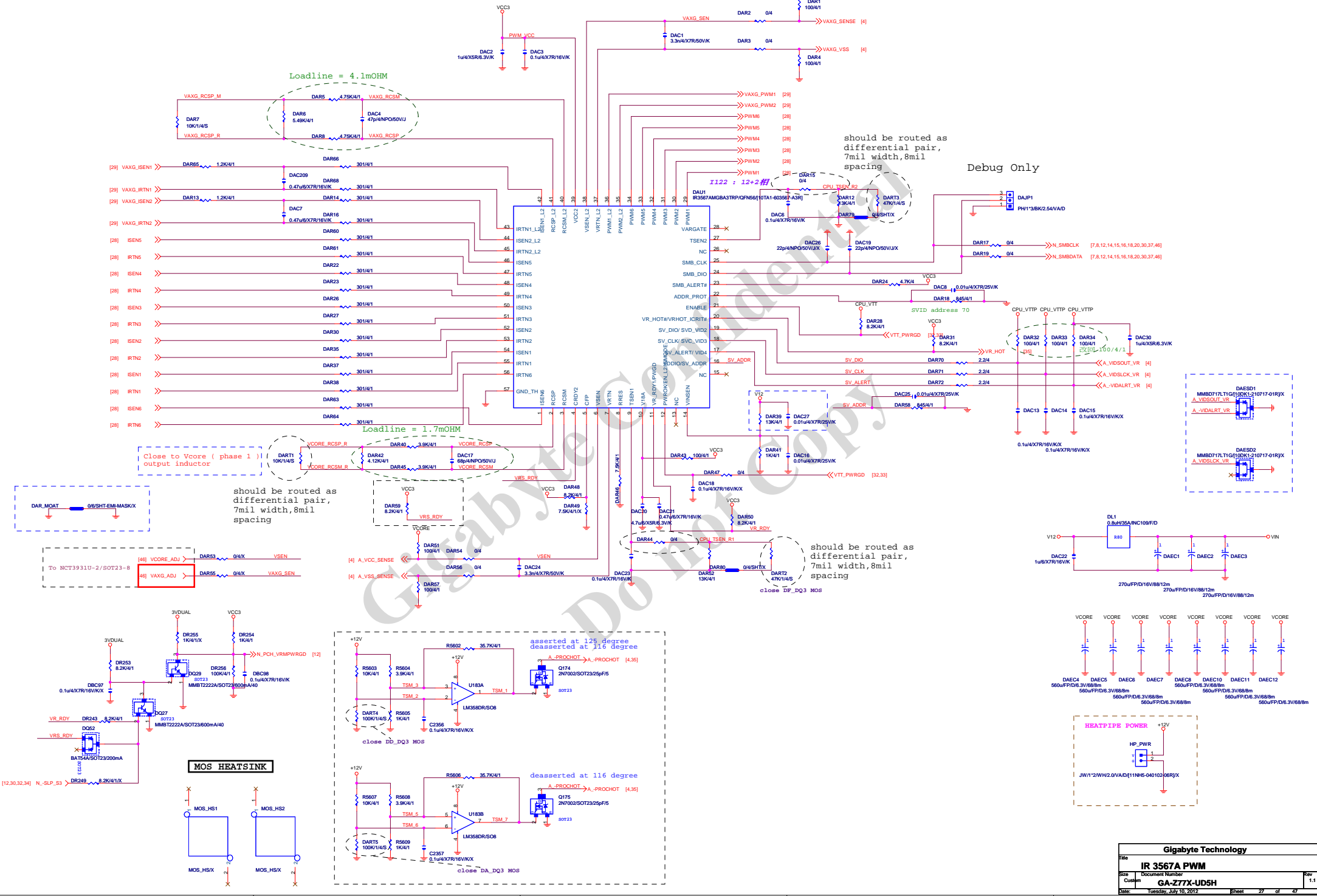
AMP\_CODEC for 889  
AMP\_CODEC1 for 898/887-VD2  
[24,25] AMP\_CODEC CR256 10K/4/X  
[24] AMP\_CODEC1 CR320 10K/4/X  
LOW : NORMAL  
HIGH : AMPLIFY  
inbox driver default low  
Realtek driver 為 high

## LINE-OUT

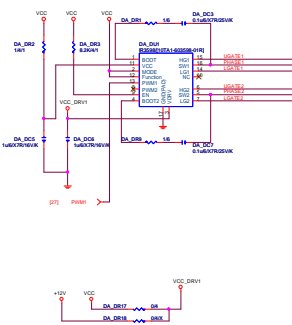
AMP\_CODEC2 CR378 470K/4/1X  
[24] AMP\_CODEC2 CR378 470K/4/1X  
LOW : NORMAL  
HIGH : AMPLIFY  
inbox driver default low  
Realtek driver 為 high



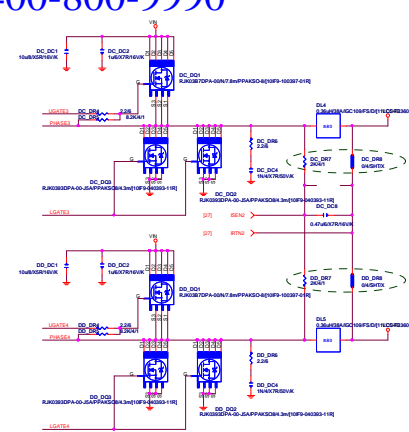
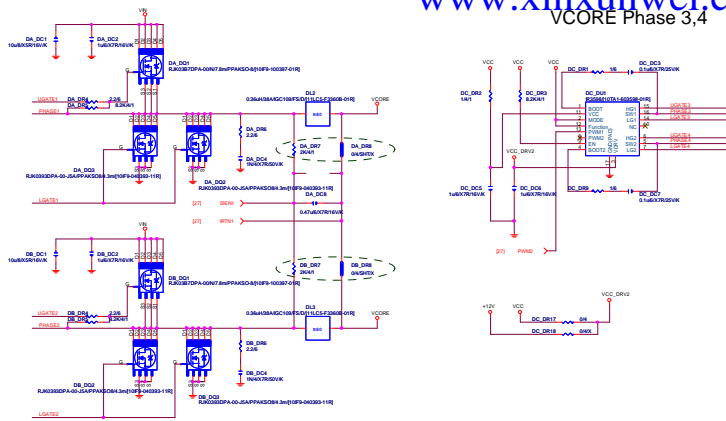




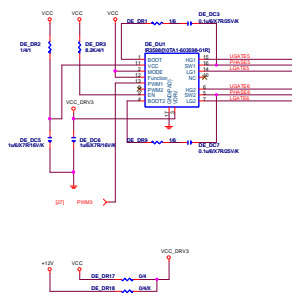
VCORE Phase 1,2



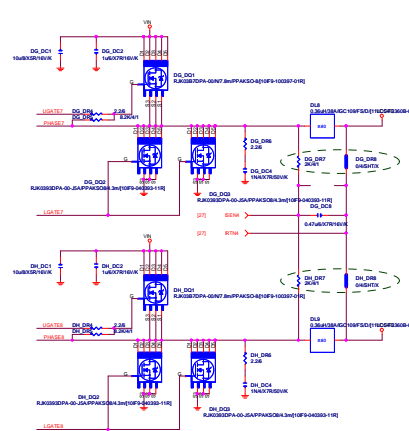
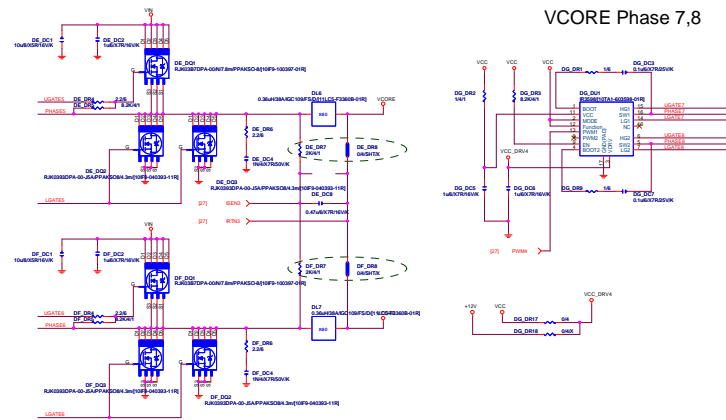
VCORE Phase 3,4



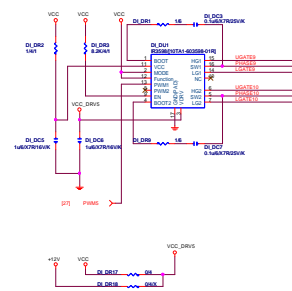
VCORE Phase 5,6



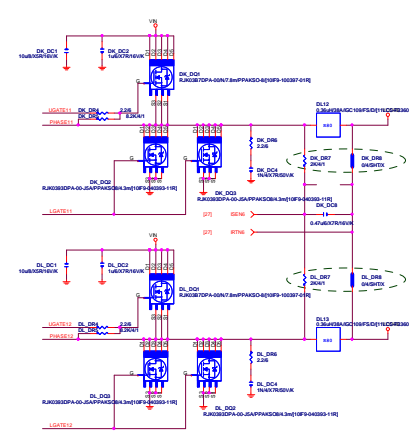
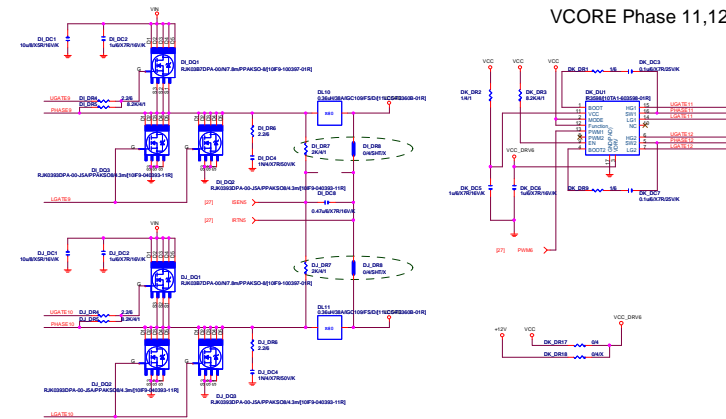
VCORE Phase 7,8



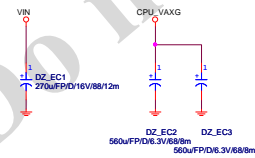
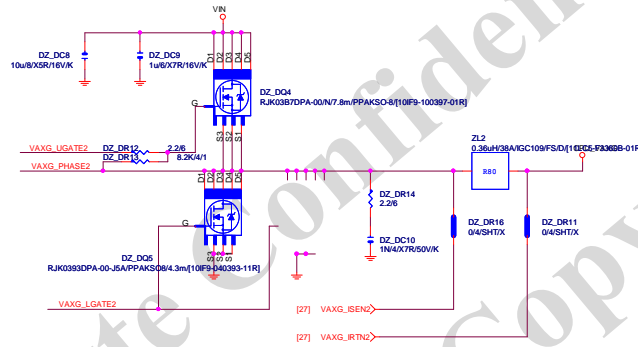
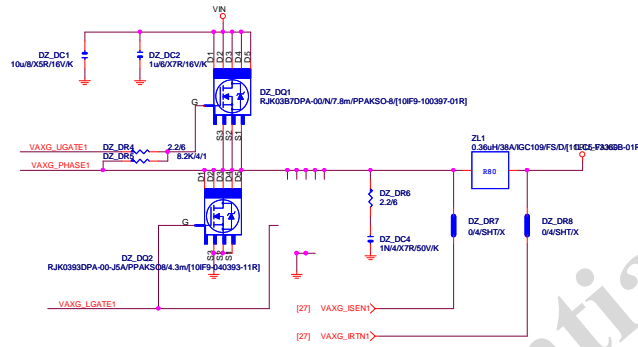
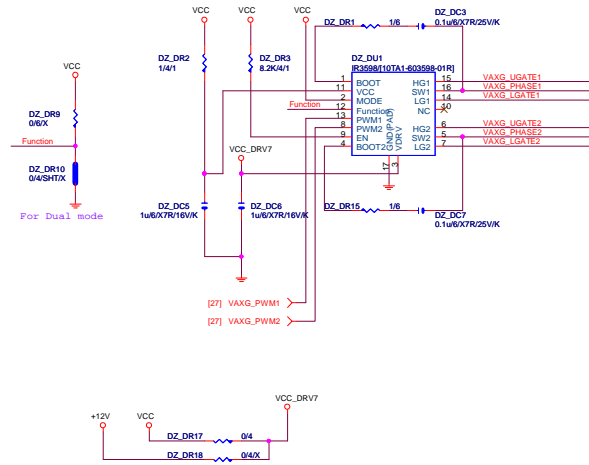
VCORE Phase 9,10

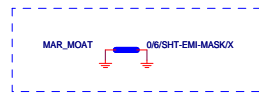


VCORE Phase 11,12

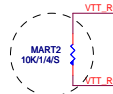


## VAXG Phase

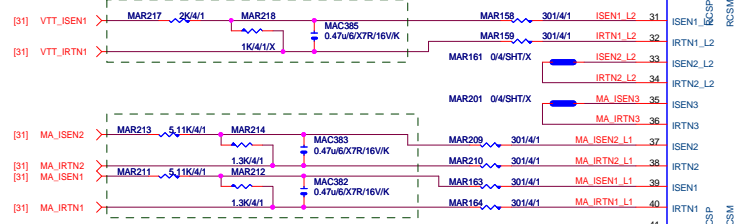
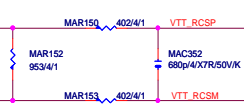




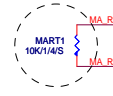
Close to VTT  
output inductor



Value need check with Vendor

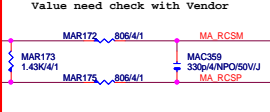


Close to DDR  
output inductor



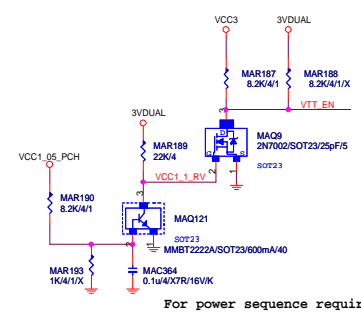
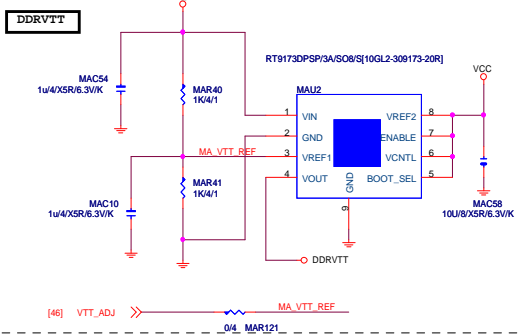
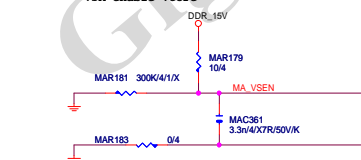
should be routed as  
differential pair,  
7mil width, 8mil  
spacing

[46] DDR15V\_ADJ1 >> MAR180 0.4SHT/X MA\_VSEN



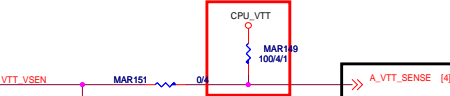
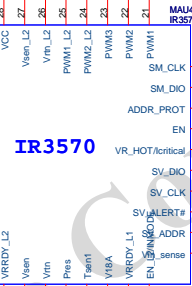
[33] CPU\_VTT\_GD << MAR205 8.2K/4/1

For power sequence ,VTT enable VSA ,then  
VSA enable Vcore

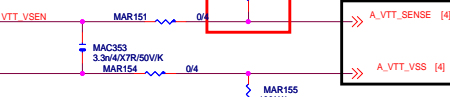


For power sequence require

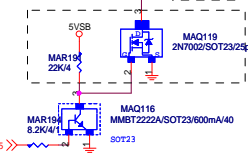
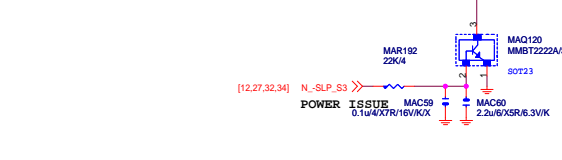
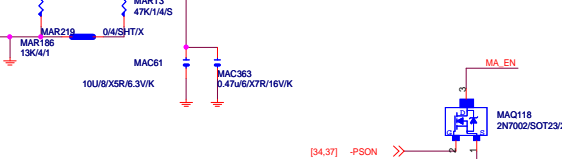
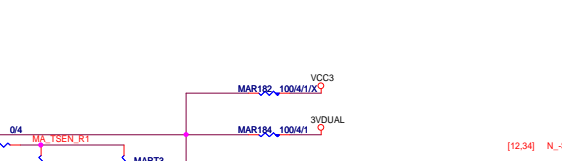
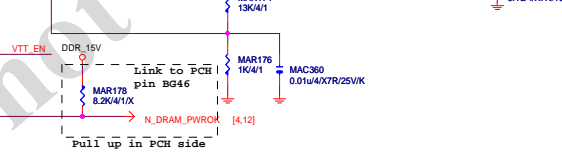
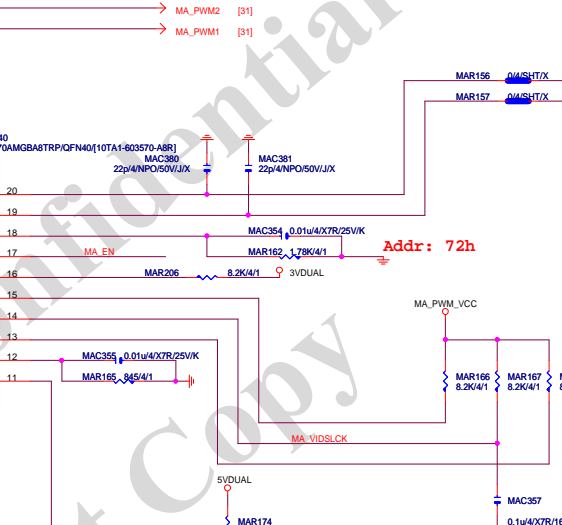
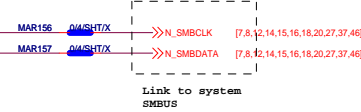
IR3570



Addr: 72h

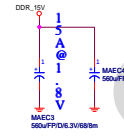
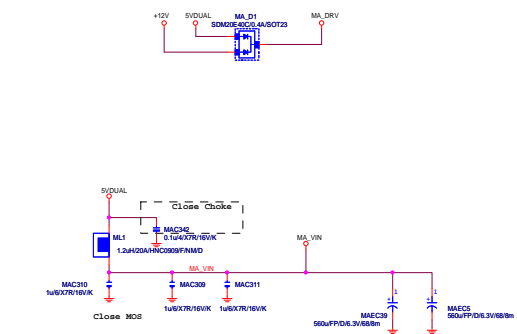


To CPU pin AB3,AB4

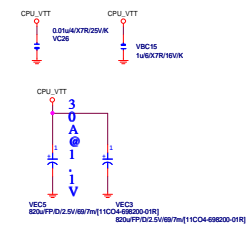
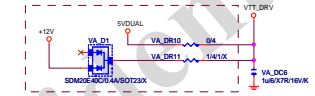


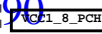
GIGABYTE™		
Title <b>DDR &amp; CPU_VTT POWER IR3570A</b>		
Size C	Document Number <b>GA-Z77X-UD5H</b>	Rev <b>1.1</b>
Date Wednesday, June 06, 2012	Sheet 30	of 47

## DDR\_15V



## CPU\_VTT





I/O ErP Control

## PCH ErP Control

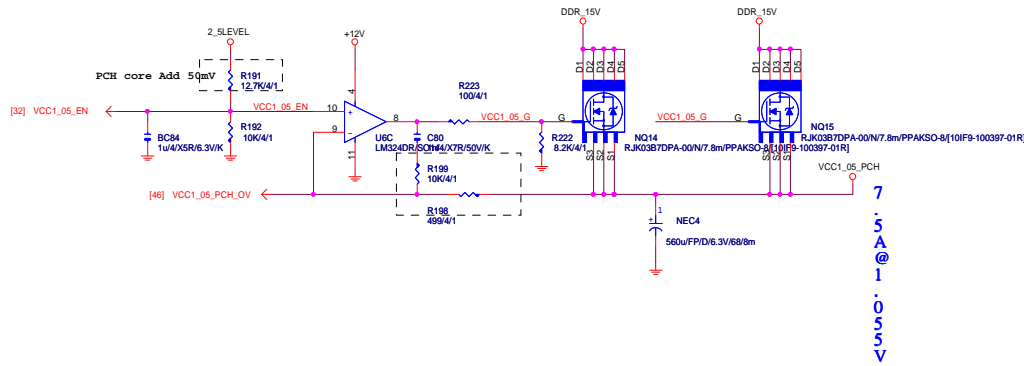
## 5VDUAL SHORT PROTECT

## Gigabyte Technology

Title			
DISCRETE POWER I			
Size	Document Number		Rev
C	GA-Z77X-UD5H		1.1
Date: Wednesday, June 06 2012		Sheet	32 of 47

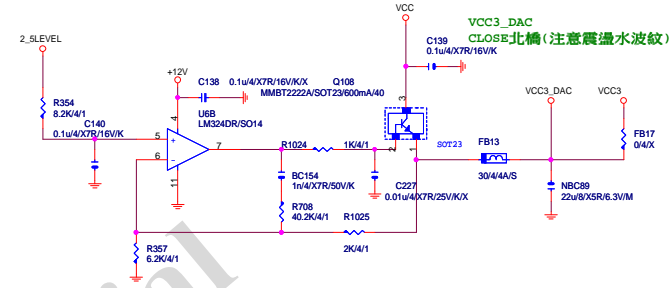


## VCC1\_05\_PCH

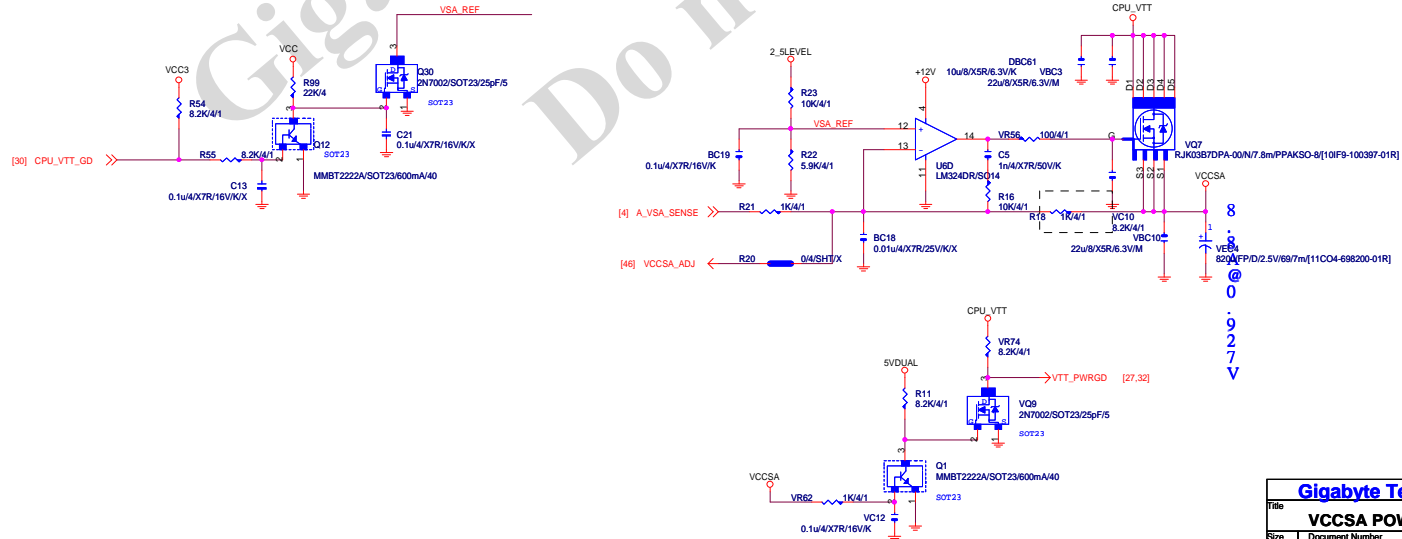


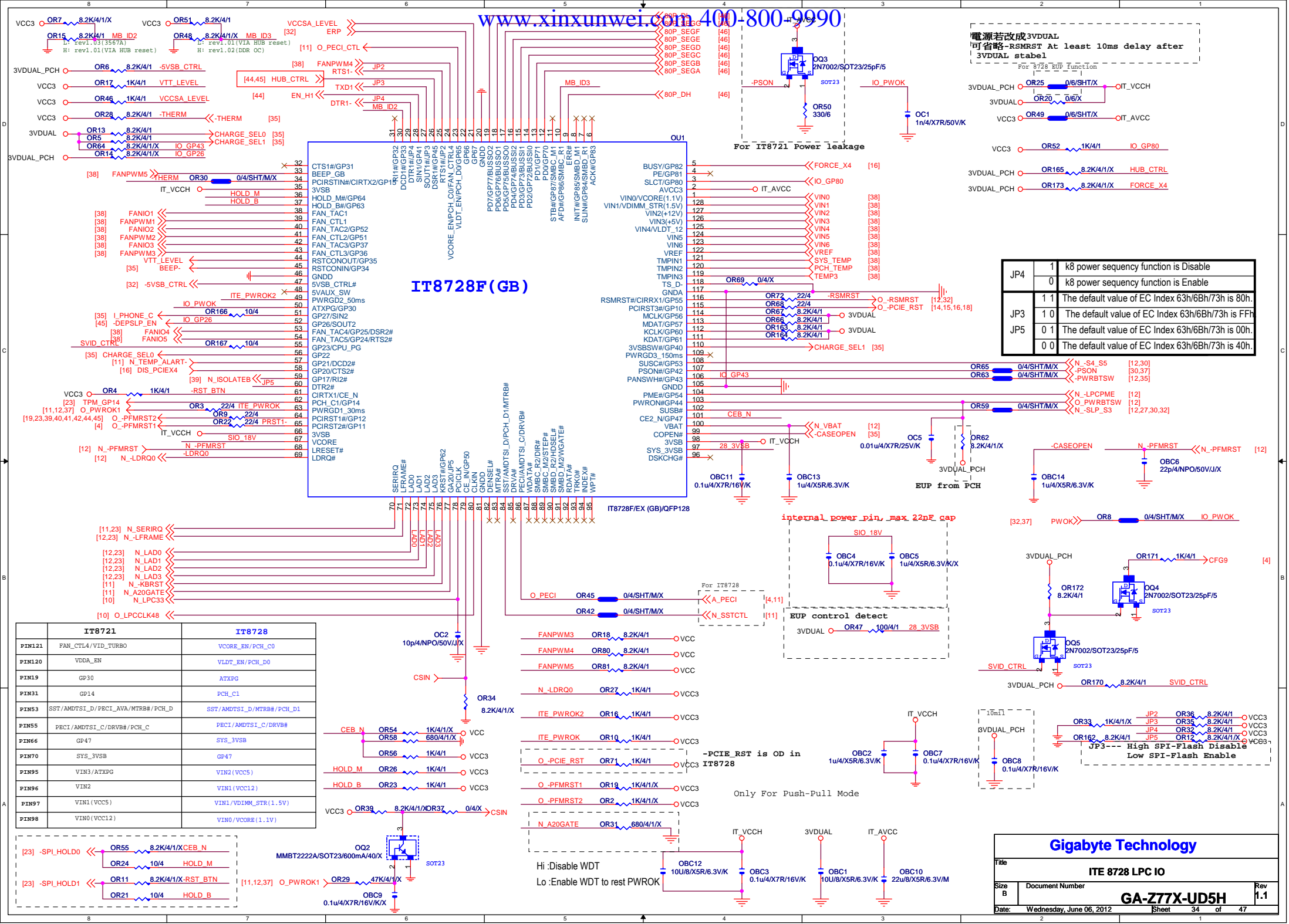
## VCC3\_DAC

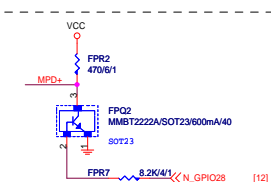
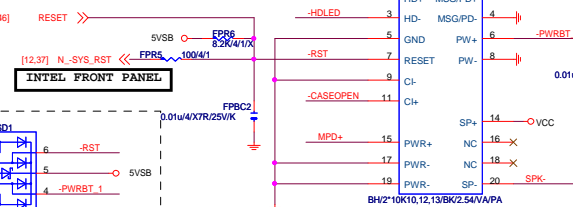
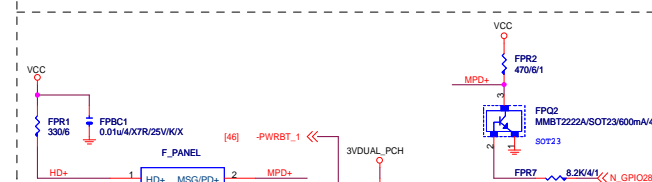
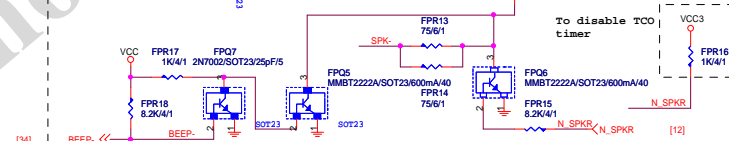
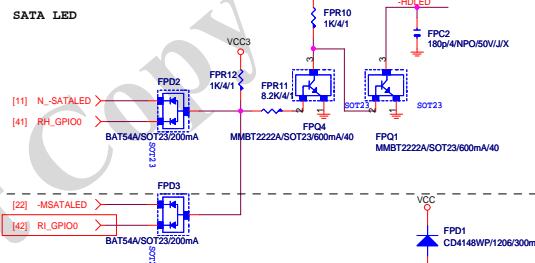
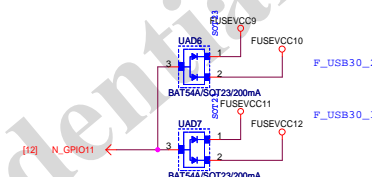
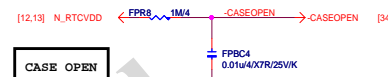
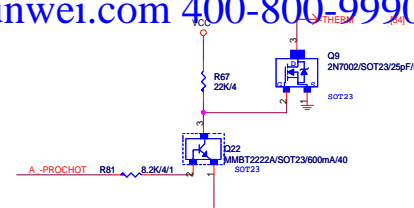
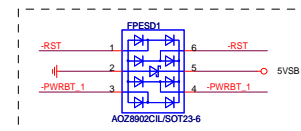
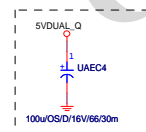
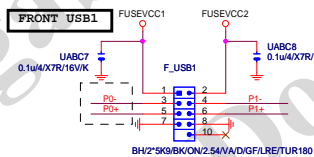
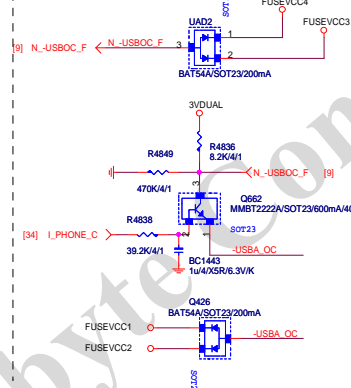
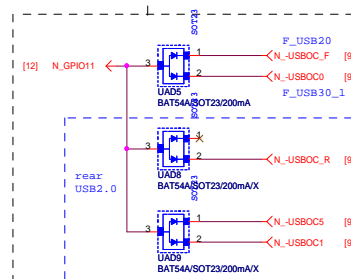
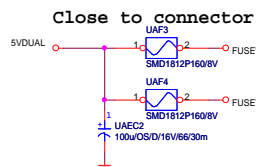
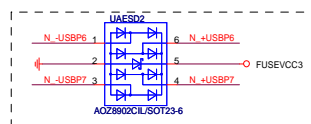
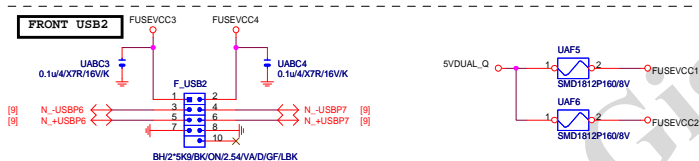
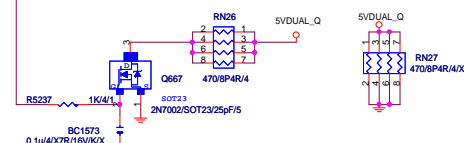
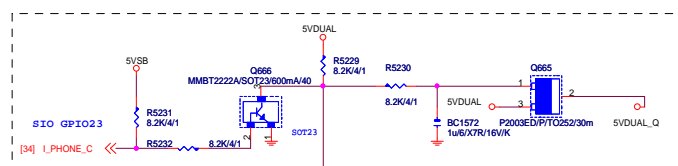
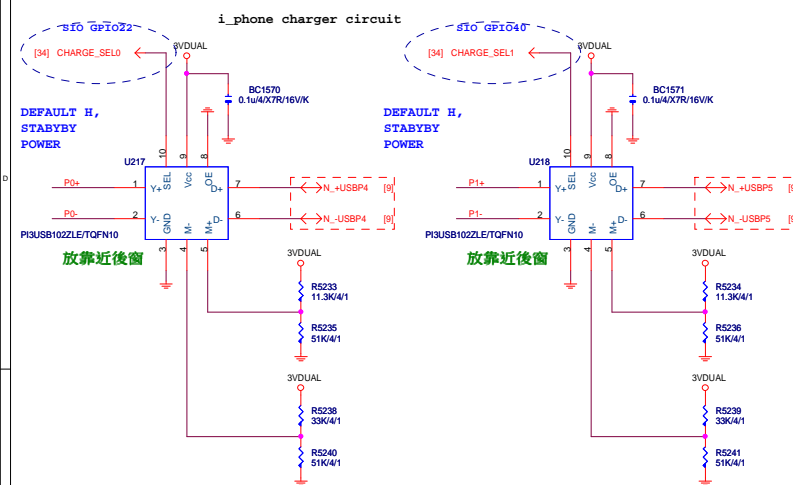
(3.3V/70mA+360uA)

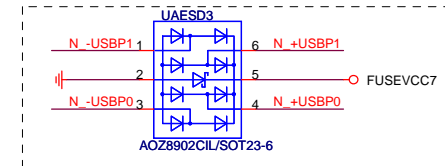
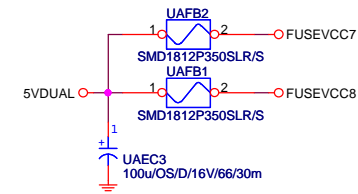
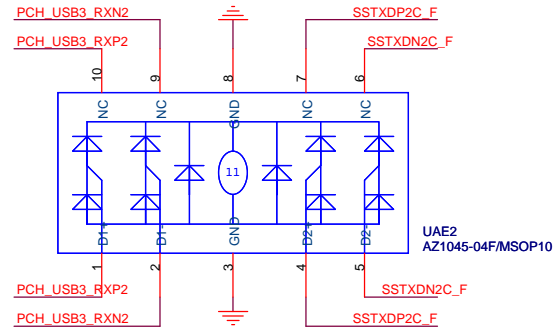
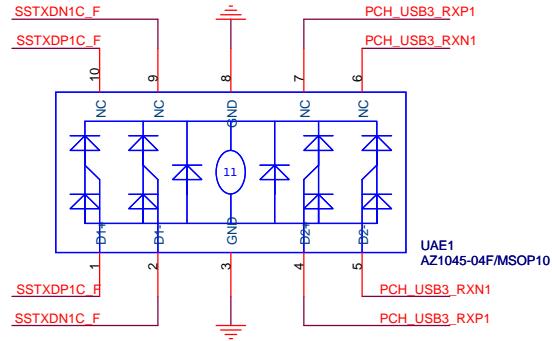
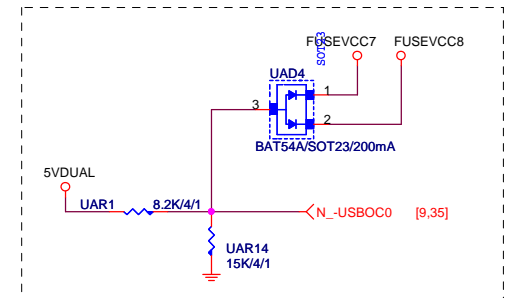
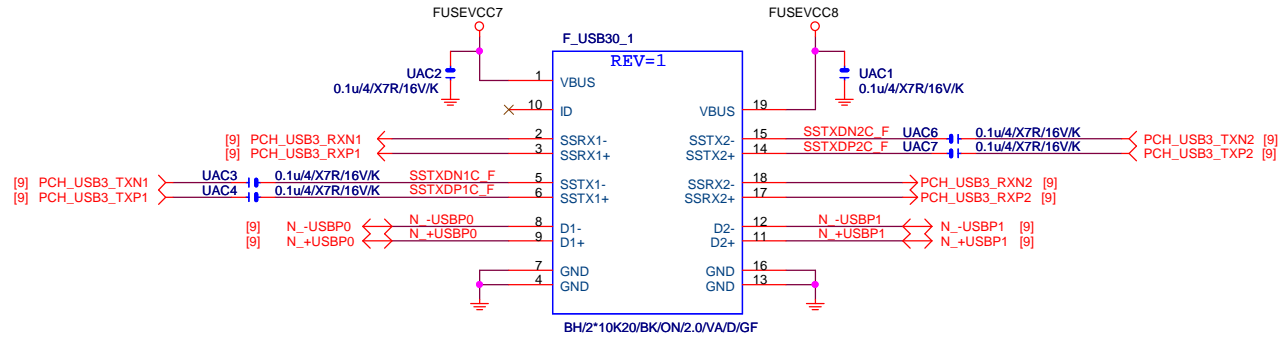


VCC\_SA





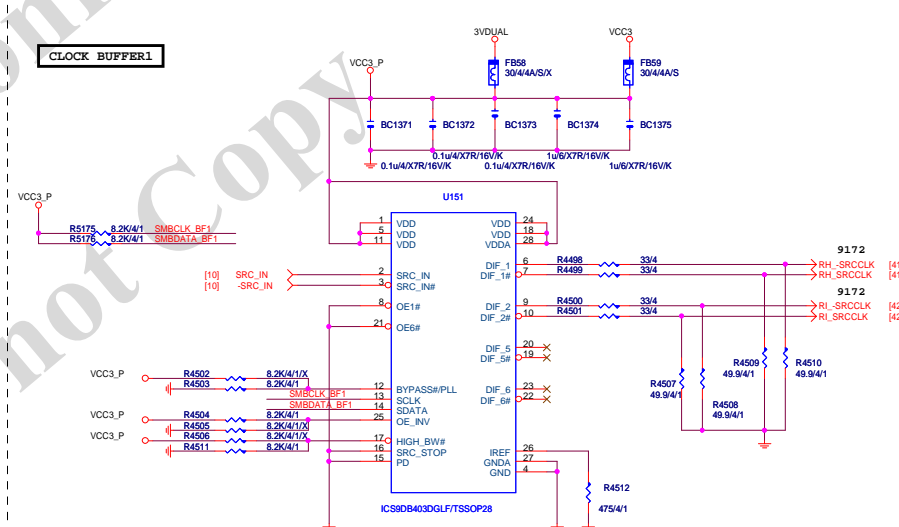
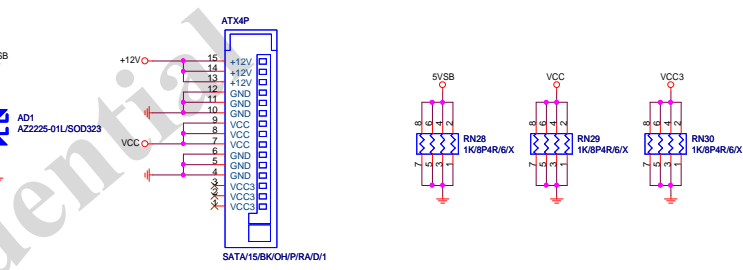




**Gigabyte Technology**

Title			
<b>F_USB 3.0</b>			
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### CPU Frequency Selection

N\_PCHCLK14 C182 10p4NPO50V/1X

CKVDD R241 8.2K/4/1/X FS 133M

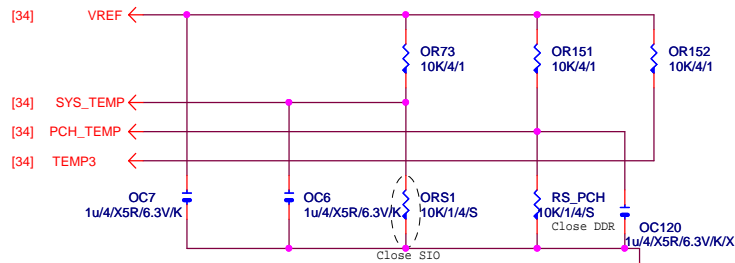
R242 8.2K/4/1

CKVDD R237 8.2K/4/1/X CPU\_STP

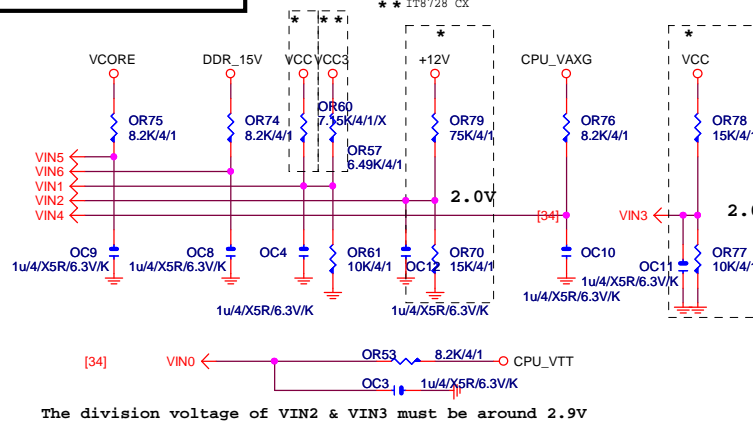
CKVDD R5384 8.2K/4/1/X LPC 48

R992 8.2K/4/1

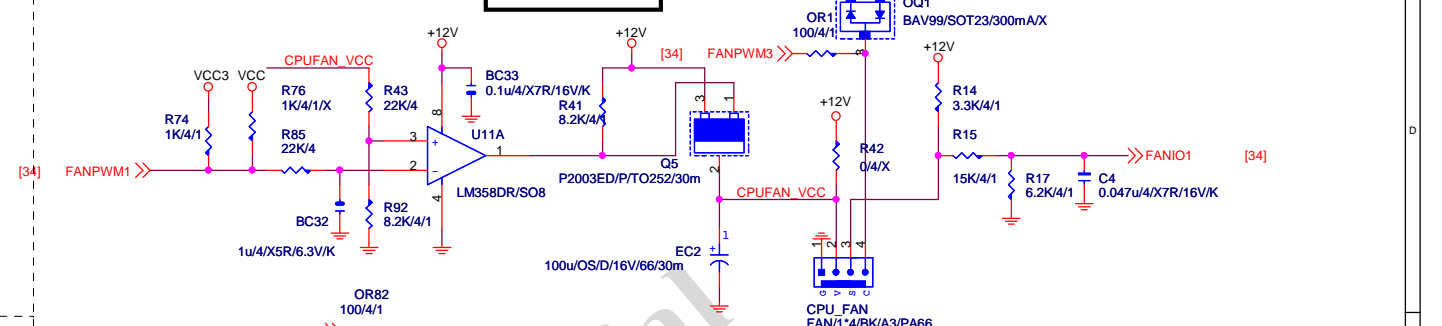
# TEMP H/W MONITOR



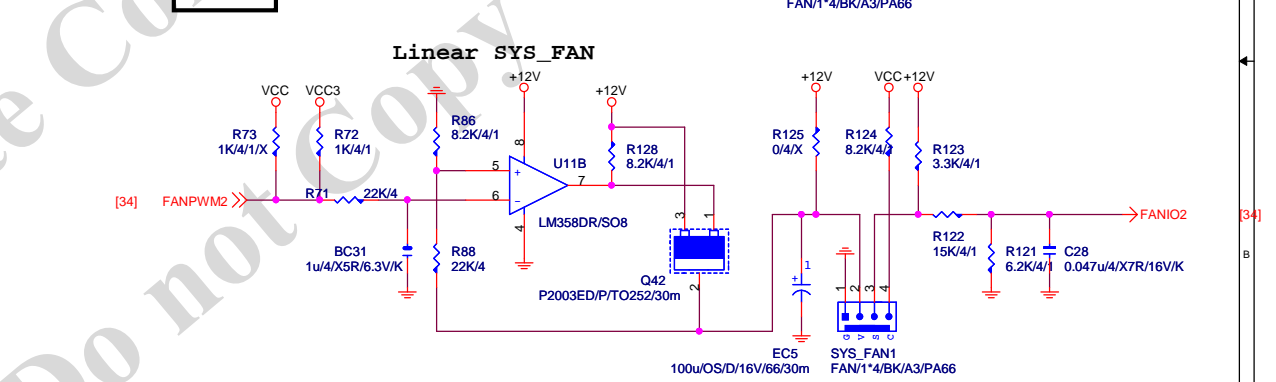
# VOLTAGE-- H/W MONITOR



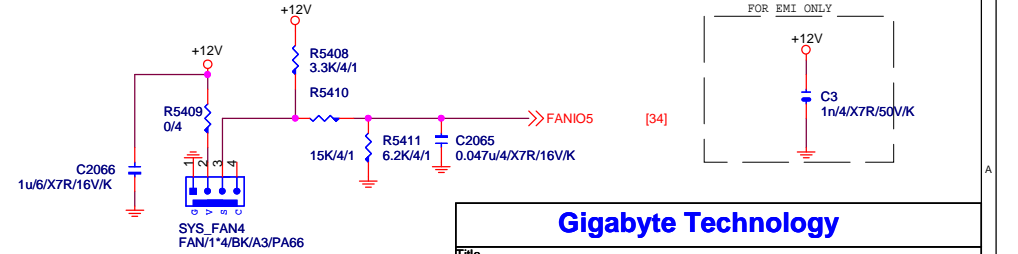
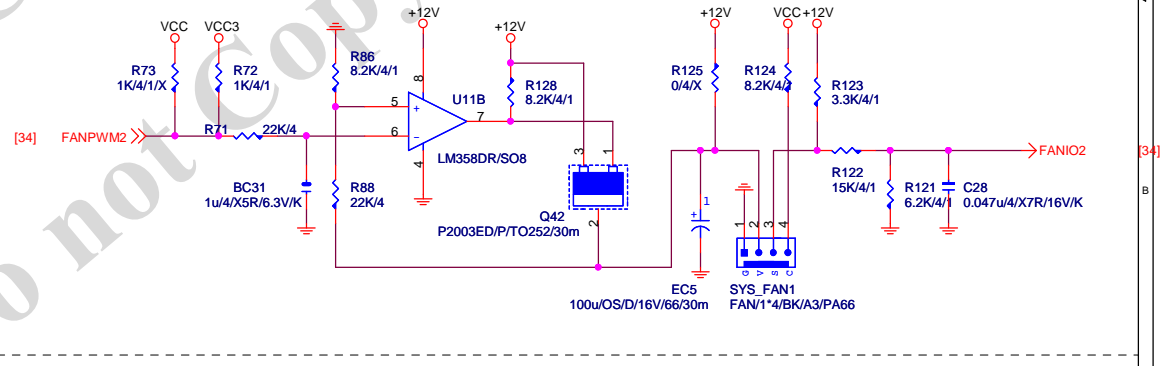
# CPU SMART FAN



# SYS FAN



# Linear SYS\_FAN

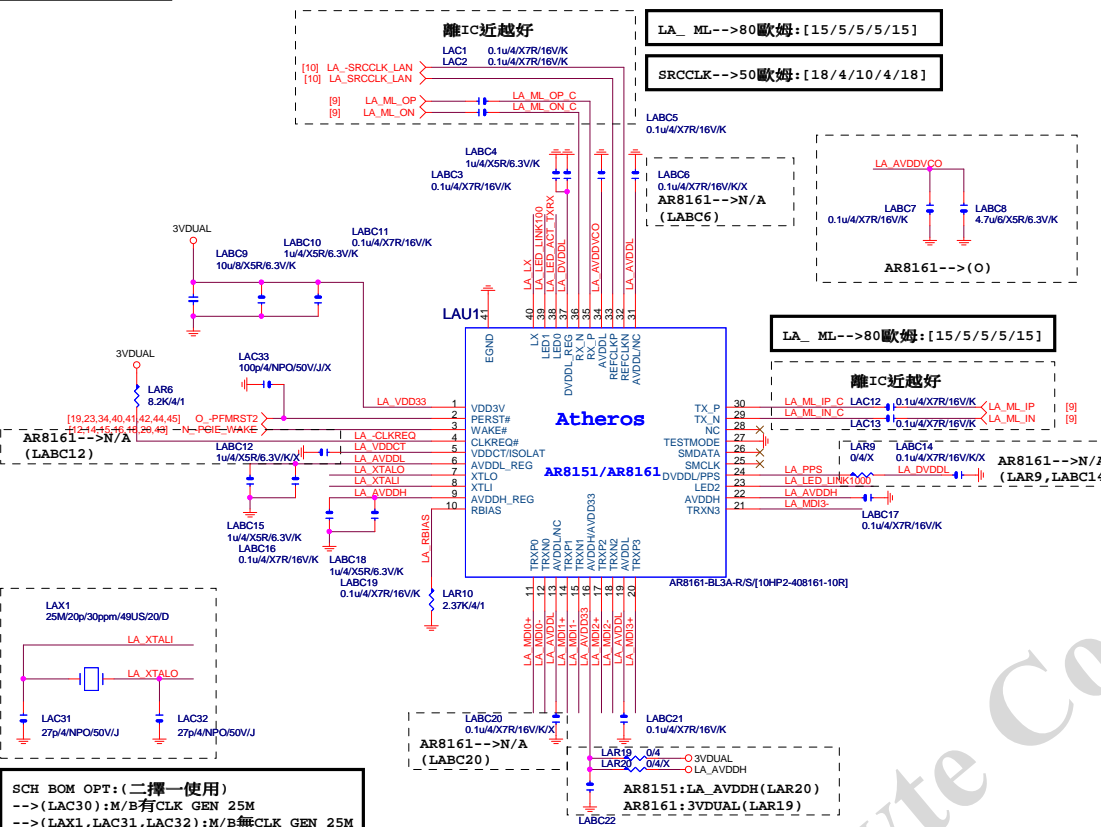


Gigabyte Technology

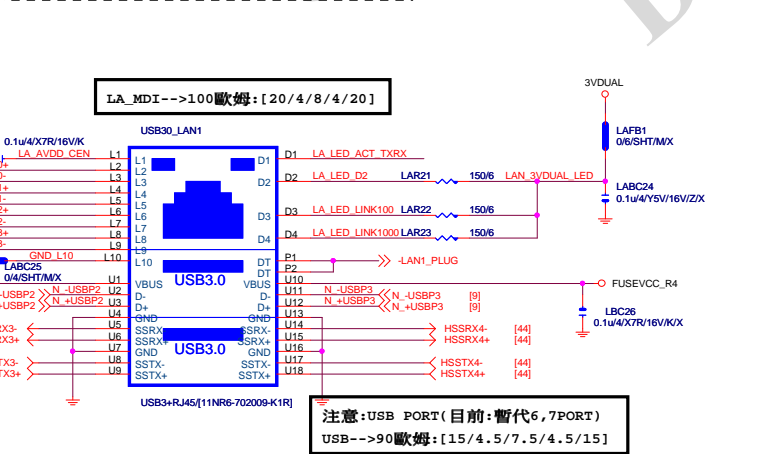
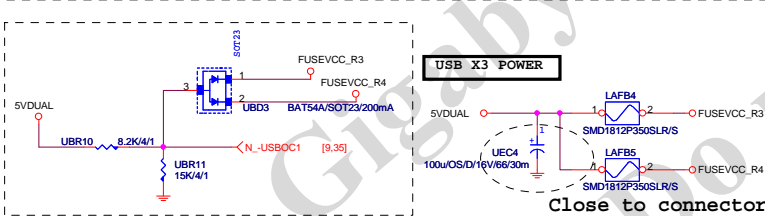
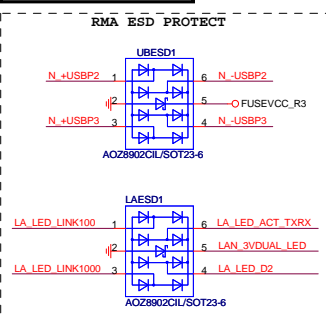
Title			
HWM,KB/MS, FAN CTRL			
Size	Document Number	Rev	
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LAN:AR8151/AR8161

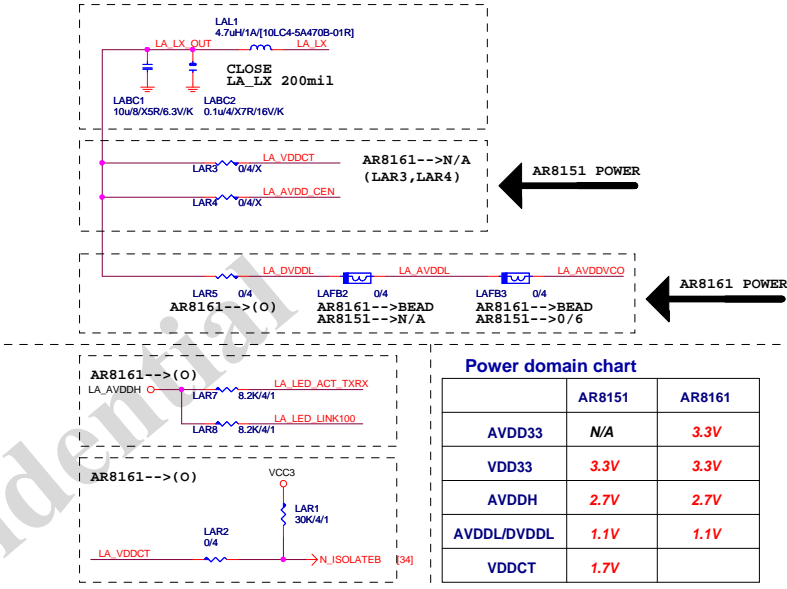


## USB\_LAN CONNECTOR

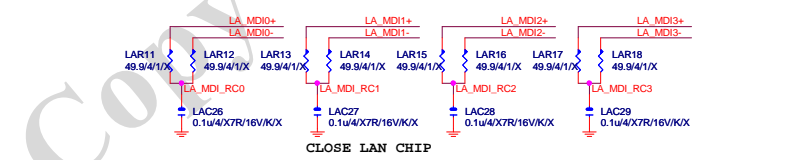


LAN POWER - NEW DESIGN ONLY FOR INTERNAL SWR

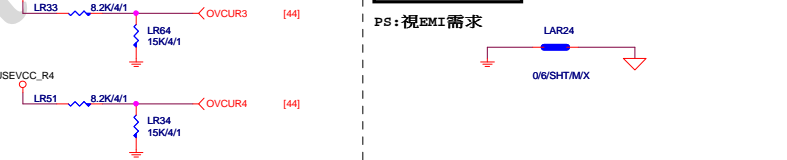
AR8151: LAR3(O), LAR5(X)  
AR8161: LAR5(O), LAR3/LAR4(X)

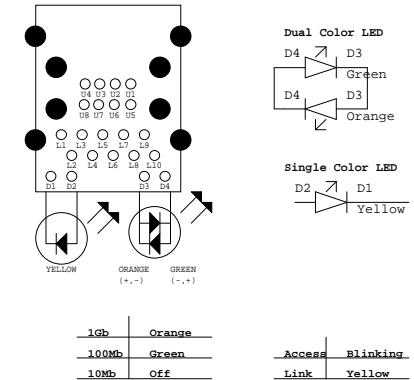
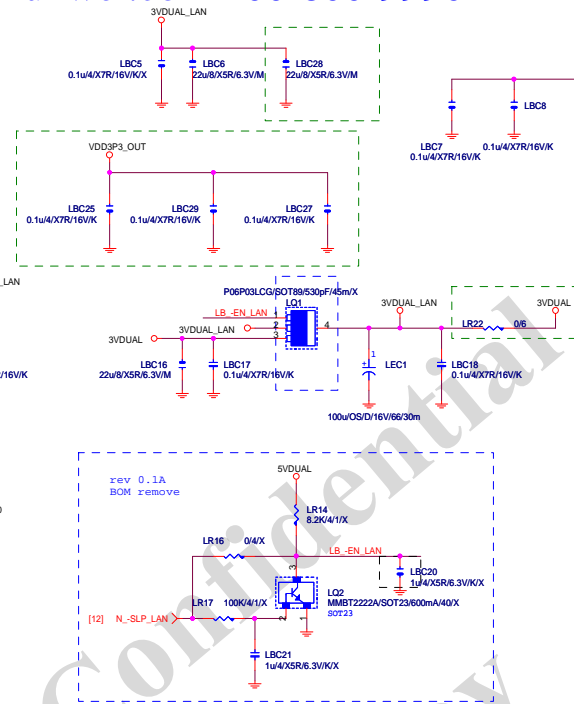
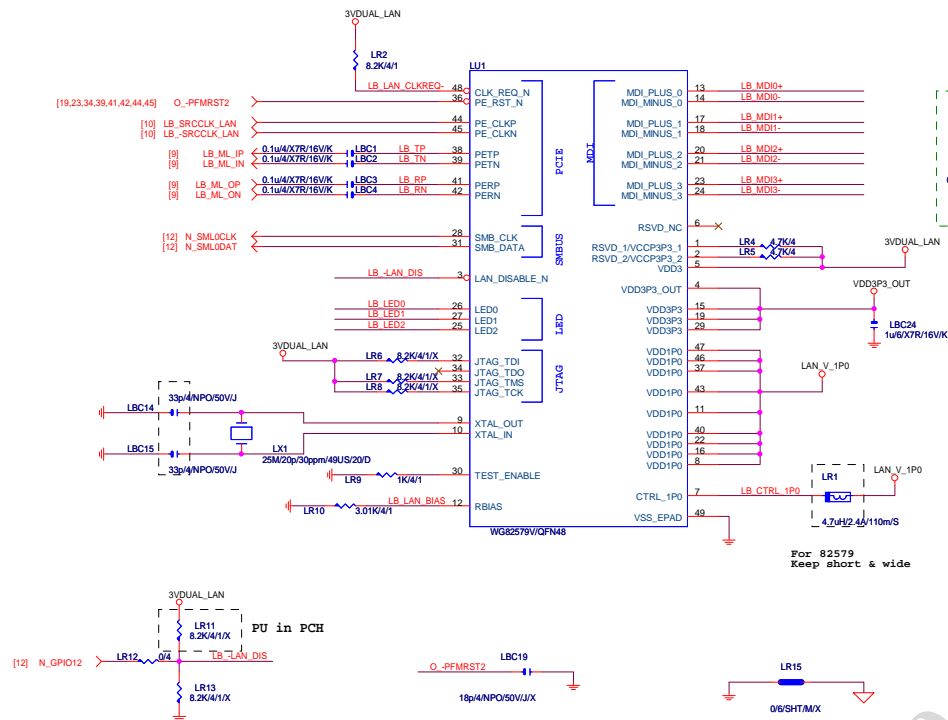


## MDI : AR8161--&gt;N/A



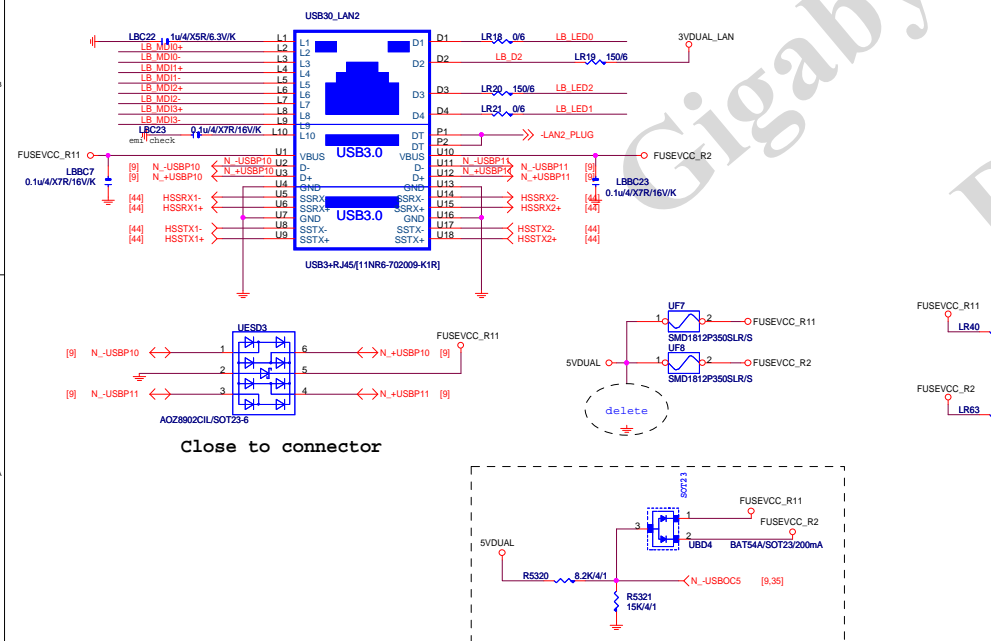
## EMI SHORT PAD



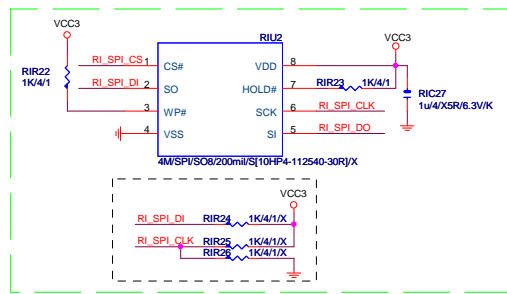
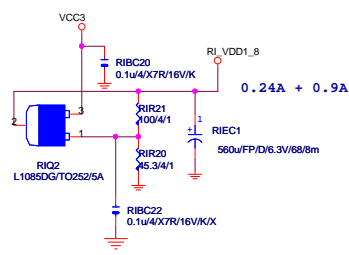
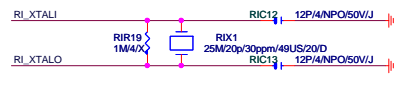
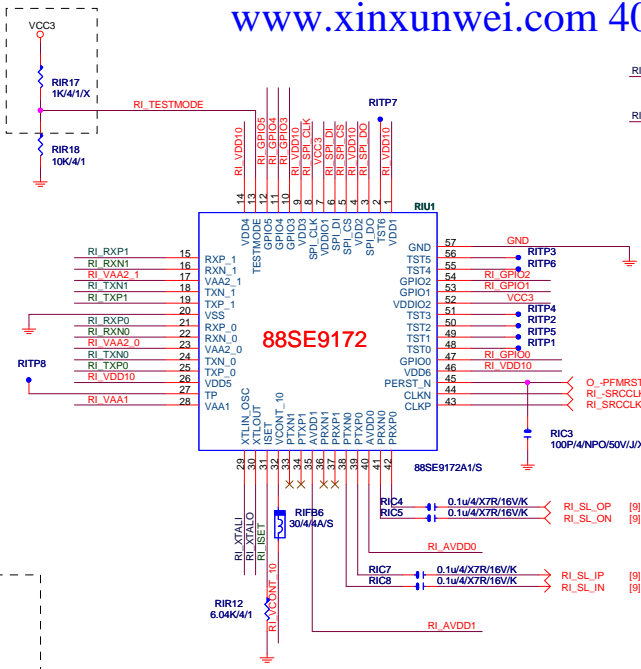
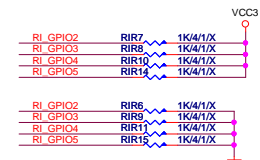
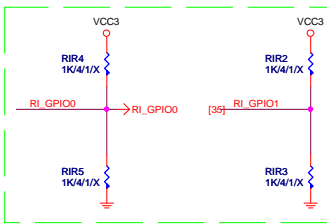
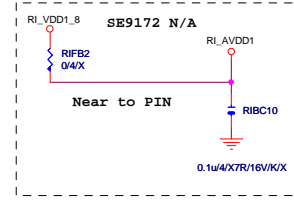
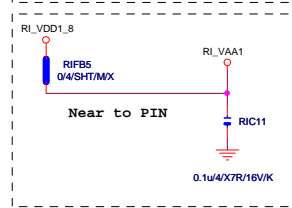
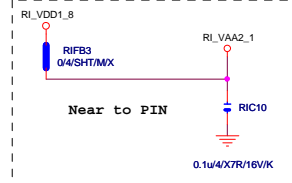
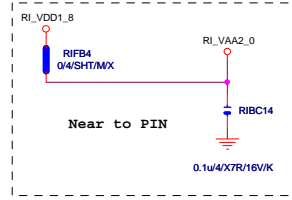
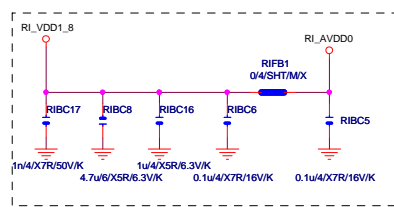
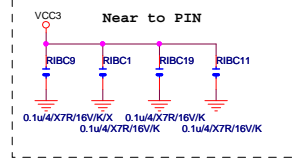
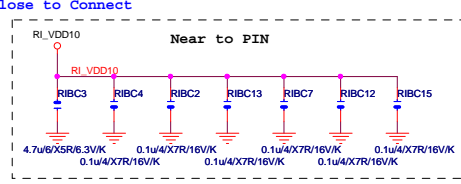


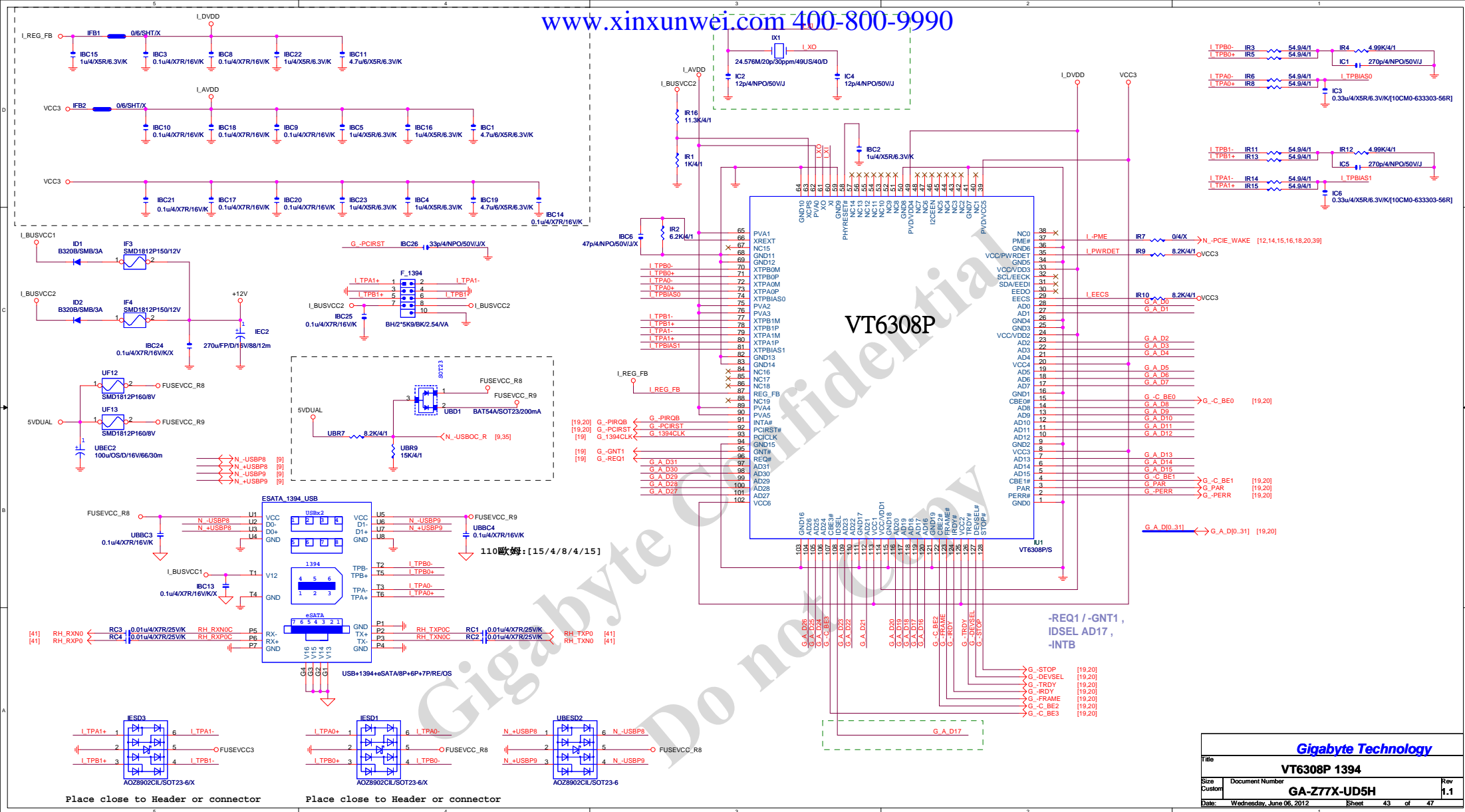
1Gb	Orange
100Mb	Green
10Mb	OFF

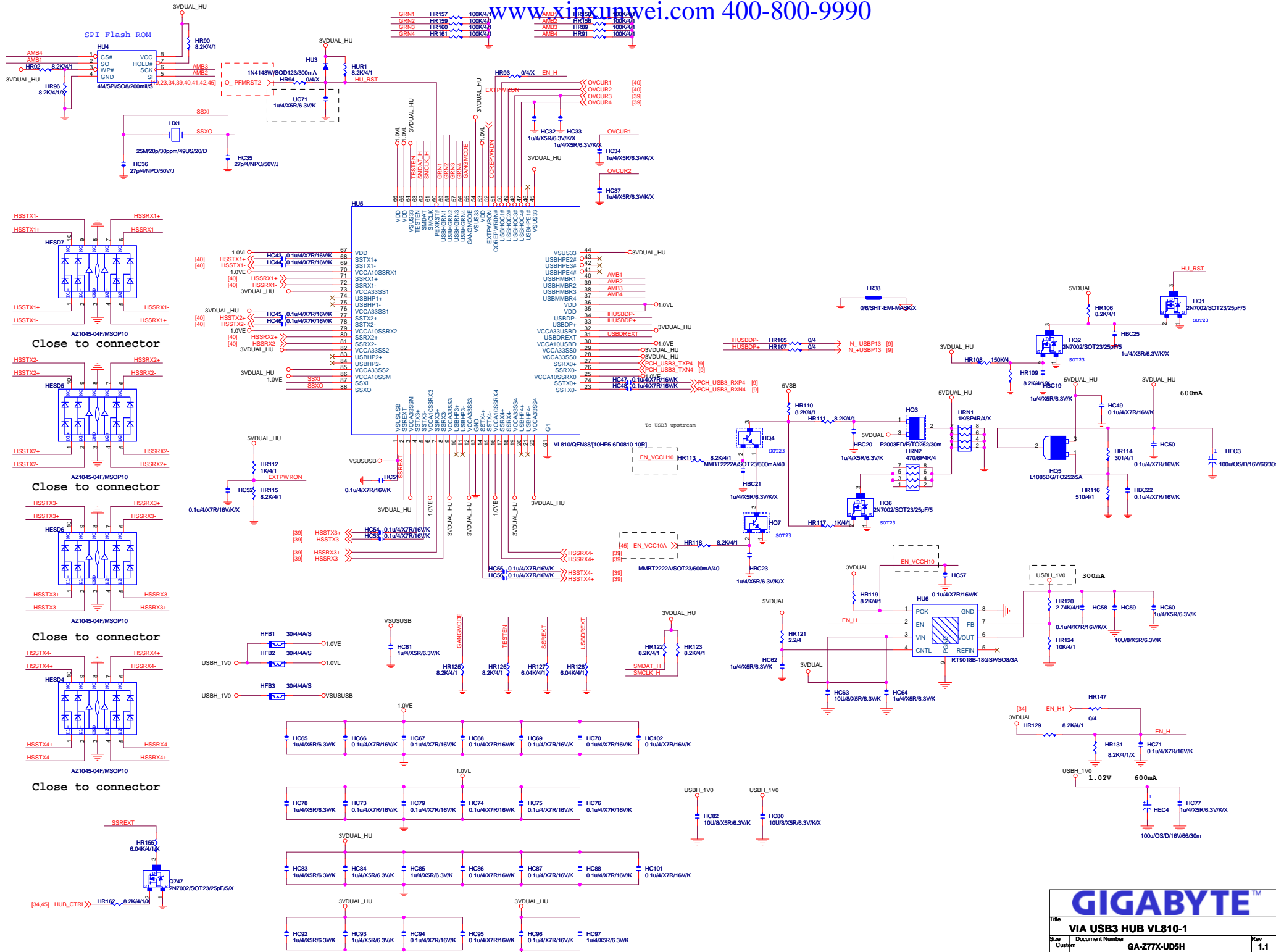
Access	Blinking
Link	Yellow



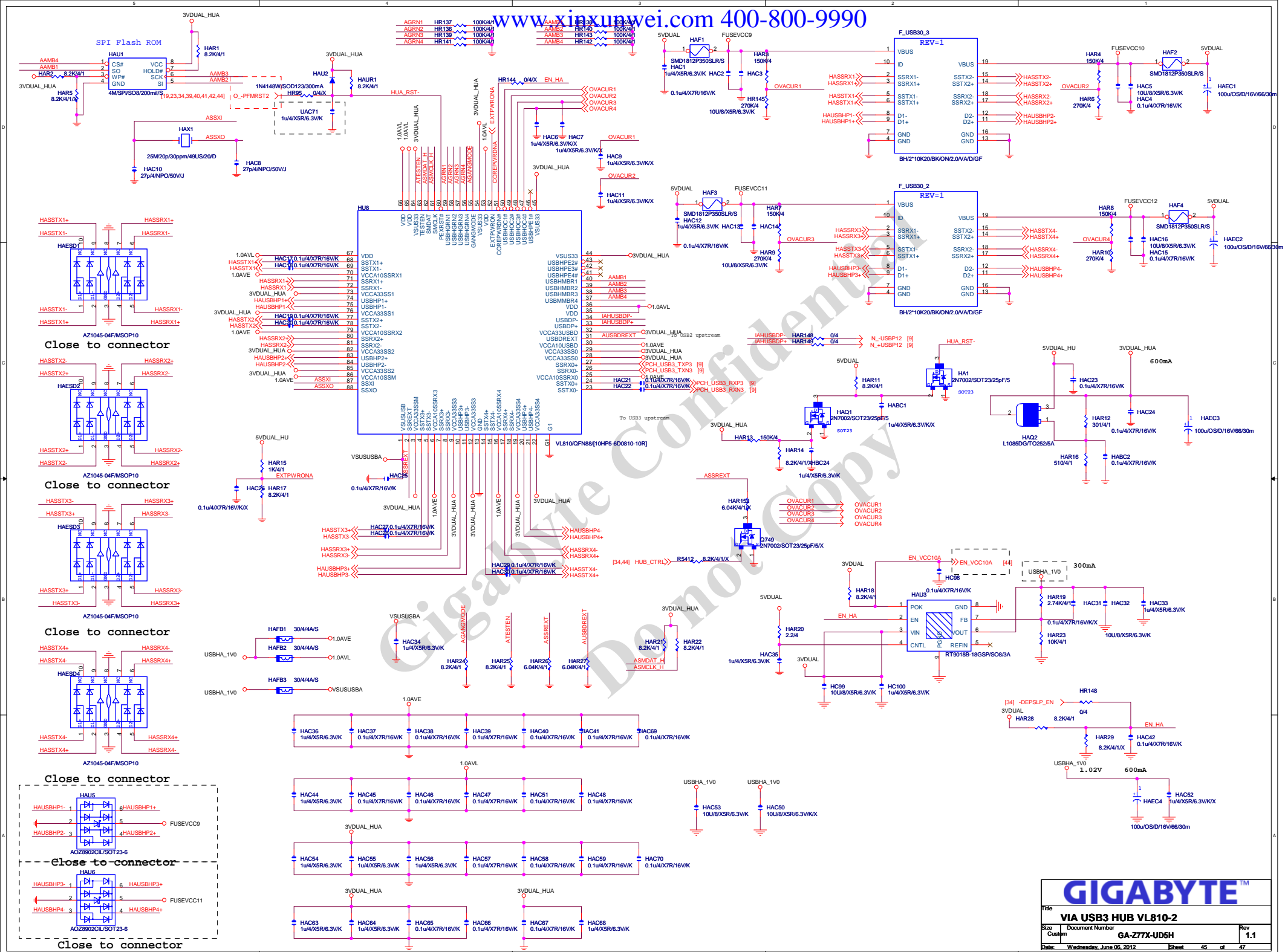














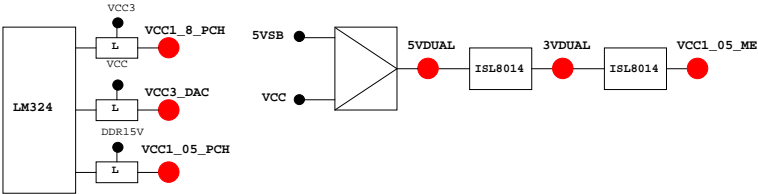


PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-AC2_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

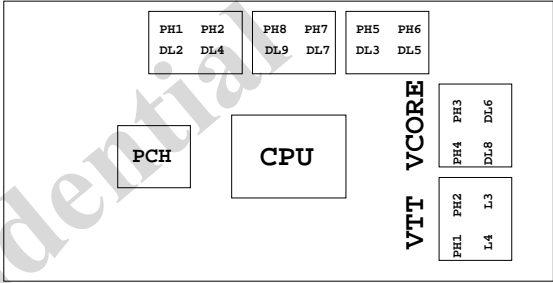
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VBSBW#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDVA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	W_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT15/CIRRXL2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_AVREF_CA_B	DRAM Address Ref
VREF_DQ_AVREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP：  
1.12SP2-01A001-Y1R/Y2R  
2.12SP2-01A001-Z1R/Z2R  
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
TABLE LIST			
Size C	Document Number	Rev	
	GA-Z77X-UD5H	1.1	
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